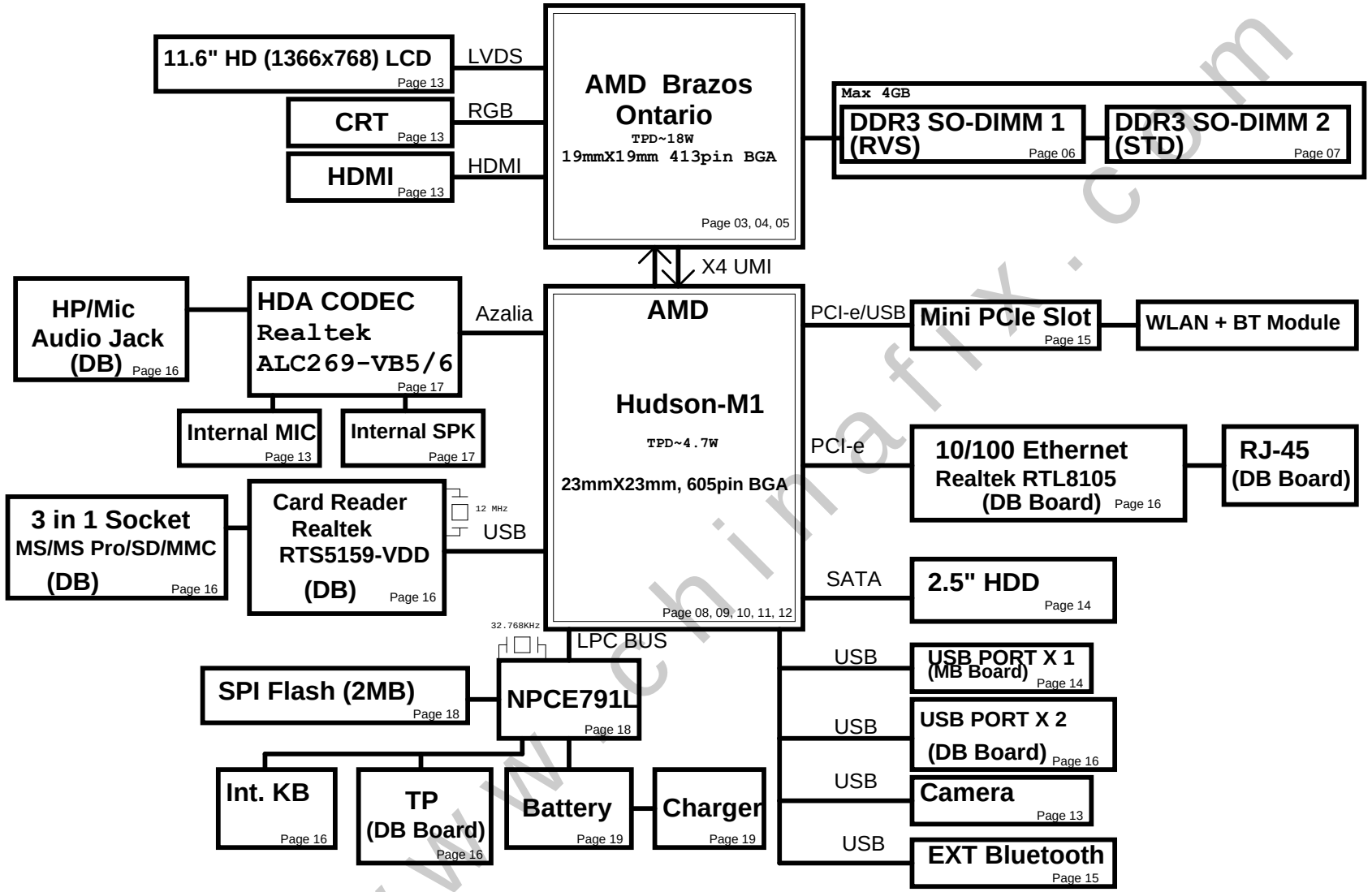
JR8 Block Diagram -- AMD Ontario



POWER

DC/DC 3V_PCU, 5V_PCU, +15V	Page 30
REGULATOR (DDR3) 1.5V_SUS, 0.75V_DDR_VTT	Page 31
REGULATOR +1V	Page 32
REGULATOR 1.1V_S5, +1.1V	Page 33
REGULATOR +1.8V	Page 34
CPU Core	Page 35
RUN POWER SW 3V_SUS, 5V_SUS, 3V_S5, 5V_S5 +3V, +5V	Page 36
Discharge	Page 36

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	System Block Diagram	2A

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Model	REV	CHANGE LIST	MODEL	JR8 FROM	JR8 To
JR8 MB	1A				
	2A	20100929 Remove Q1, R73, R64, R65 Change CN10 P/N from DFHS02FS340 t0 DFHS02FS027 20101004 Add CL1, CL2 Remove JP1, JP3, JP4, JP5, JP7, JP8, JP9, JP10, JP11, JP12, JP14, JP13, JP15, JP16 Change PR130 to 0ohm PR131, PC66, PC67, PC113, PR103, PR134, PC98, PC14上件 Change PR6, PR7, PR114, PR115 P/N from CS05003F910 to CS04993F953 Change C35, C41, C45, C69, C76, C78, C83, C96, C98, C109 C134 P/N from CH1184J0b00 to CH11806JB09 Change U14 P/N from AJ079200T03 to AJ079200T04 Change PR11 from 6.2kohm to 8.2kohm Change PR165, PR153 from 174kohm to 150kohm Change PR59 from 0kohm to 200kohm Change PR113 from 0kohm to 430kohm Change C343 from 100uF to 150uF Change C339 from 1uF to 220pF Change C340 from 4.7uF to 220pF Change C342 from 0.1uF to 220pF Add R329, R330, R331 for EMI reserved 20101005 Change CL1, CL2 type Addtional C352, C353 for EMI Remove JP2, JP6 20101006 Change +1V to +1.05V Change C12, C13 from 33pF to 1000pF 20101007 Remove Hole11, Hole12 Remove CN18 Add J2~J28 Test Point Remove C57, C101 Connect CN15.13,14 connect to GND Change PC66, PC67, PC113 from 15uF to 100uF PC3不上件, PC26上件 20101007 PR131, PC31不上件 Change PU1 P/N to AL008380001 Change C330, C333 from 22pF to 18pF Change C269不上件 Change L1, L2, L3 from CX8BA750006 to CX8BA470003			

Quanta Computer Inc. PROJECT : JR8	DOC NO.	PROJECT MODEL : JR8	APPROVED BY:	DATE:	2010/09/29
Size / Document Number: Change list / Rev		PROJECT NUMBER:	REVIEWED BY:	REVISON:	2A
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5	ONTARIO POWER & DECOUP(3/3)	
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7	DDR3 SO-DIMM (STD)	
8	HUDSON PCIE/LPC/CPU IF(1/5)	
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11	HUDSON PWR/GND(4/5)	
12	HUDSON STRAPS/PWRGD(5/5)	
13	LCD/CAMERA	
14	CRT CONN	
15	LAN(RTL8103EL/8111DL)	
16	AUDIO (CX20582, SPK)	
17	SATA	
18	USB x 3	
19	Card Reader-RTL5159	
20	WLAN	
21	WWAN	
22	KB/TP	
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24	FAN/Thermal	
25	SW/LED/RFID_EEPROM	
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28	Power Diagram	
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31	DDR3(UP6163BQAG)	
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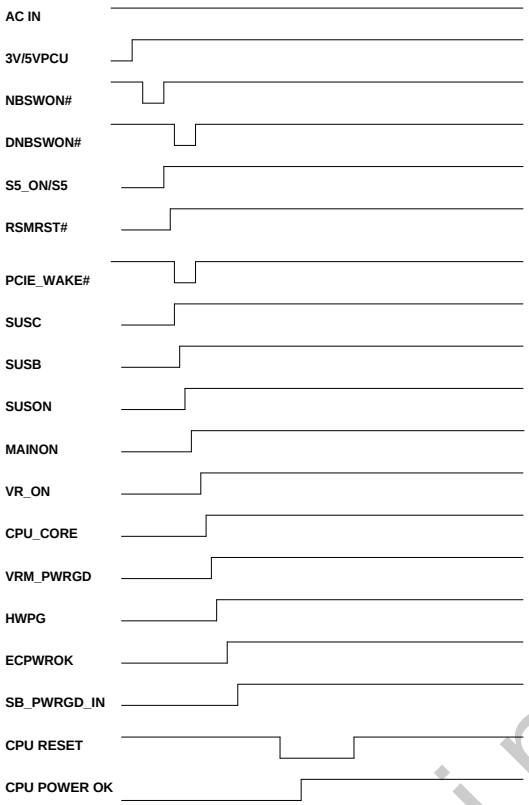
Power Sequence



Hudson M1 SM BUS

SB820 SMBUS	Pin NO.	SMBUS Function Define
PCLK_SMB PDAT_SMB (+3V)	AD22 AE22	DDR / RFID
SB_SMBCLK1 SB_SMBDATA1 (+3V_S5)	F5 F4	not used
SB_SCLK2 SB_SDATA2 (+3V_S5)	D25 F23	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used

KBC(EC) SM BUS

KBC SMBUS	Pin NO.	SMBUS Function Define
MBCLK MBDATA (+3VPCU)	110 111	Battery
MBCLK_THRM MBDATA_THRM (+3VPCU)	115 116	Thermal

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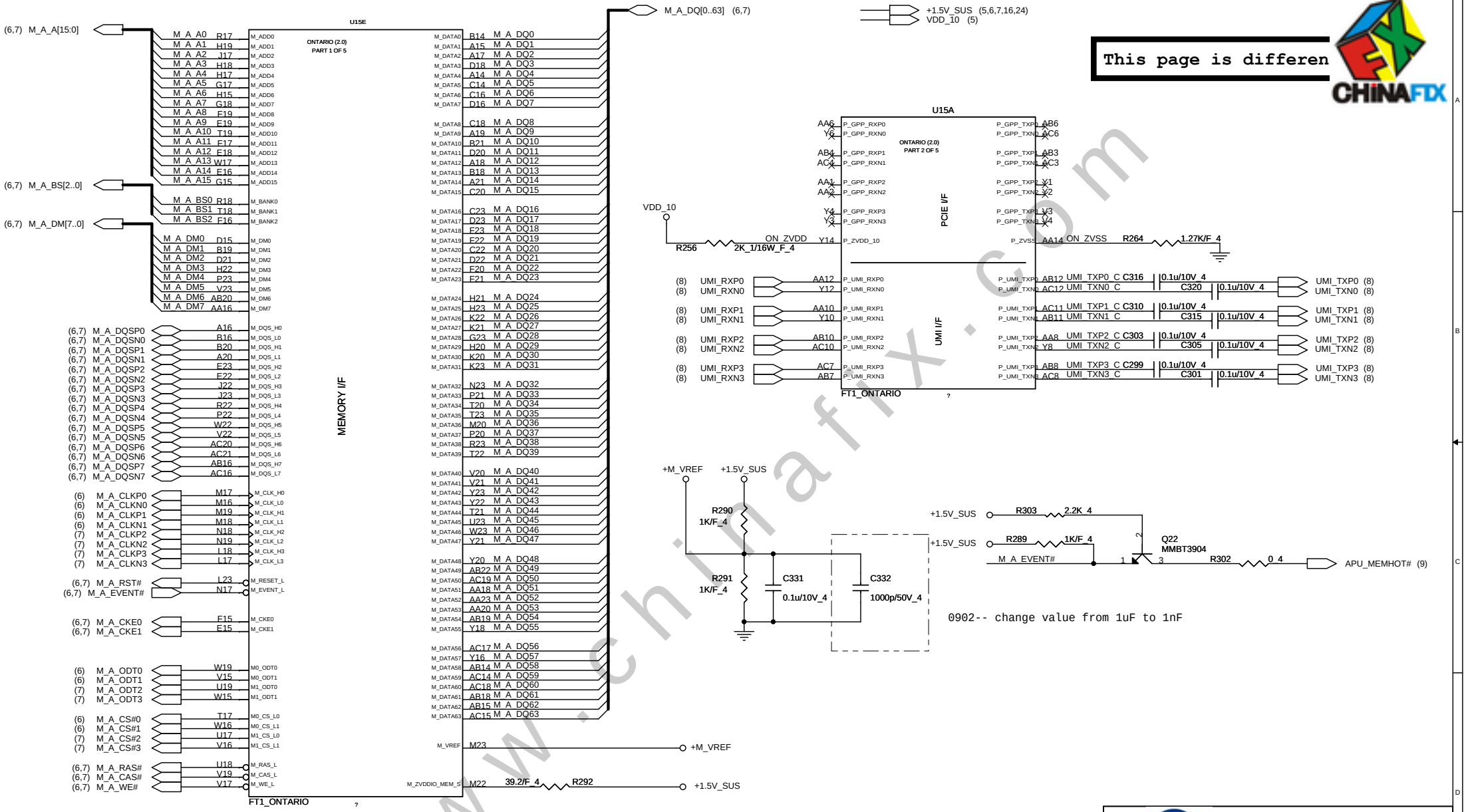

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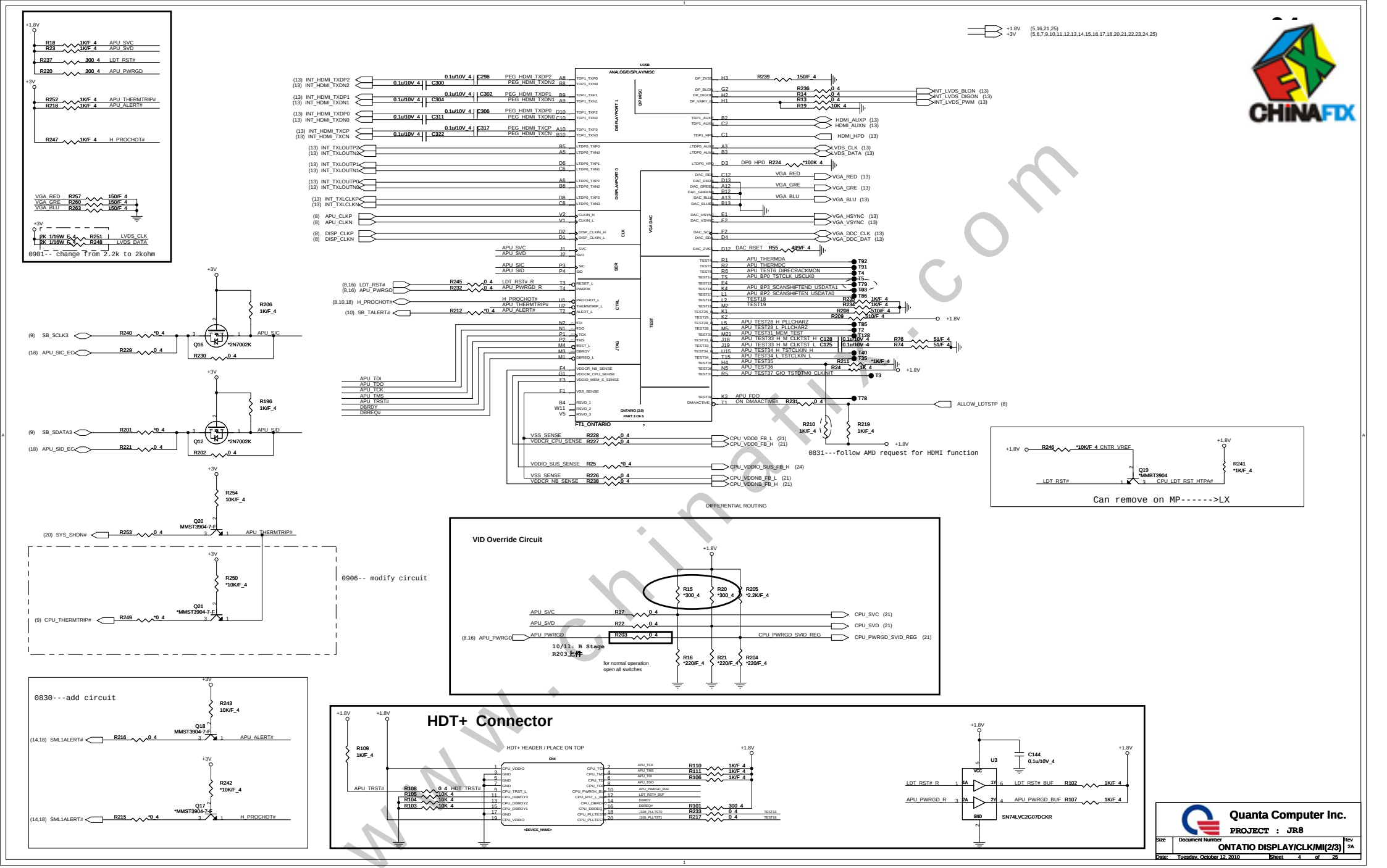

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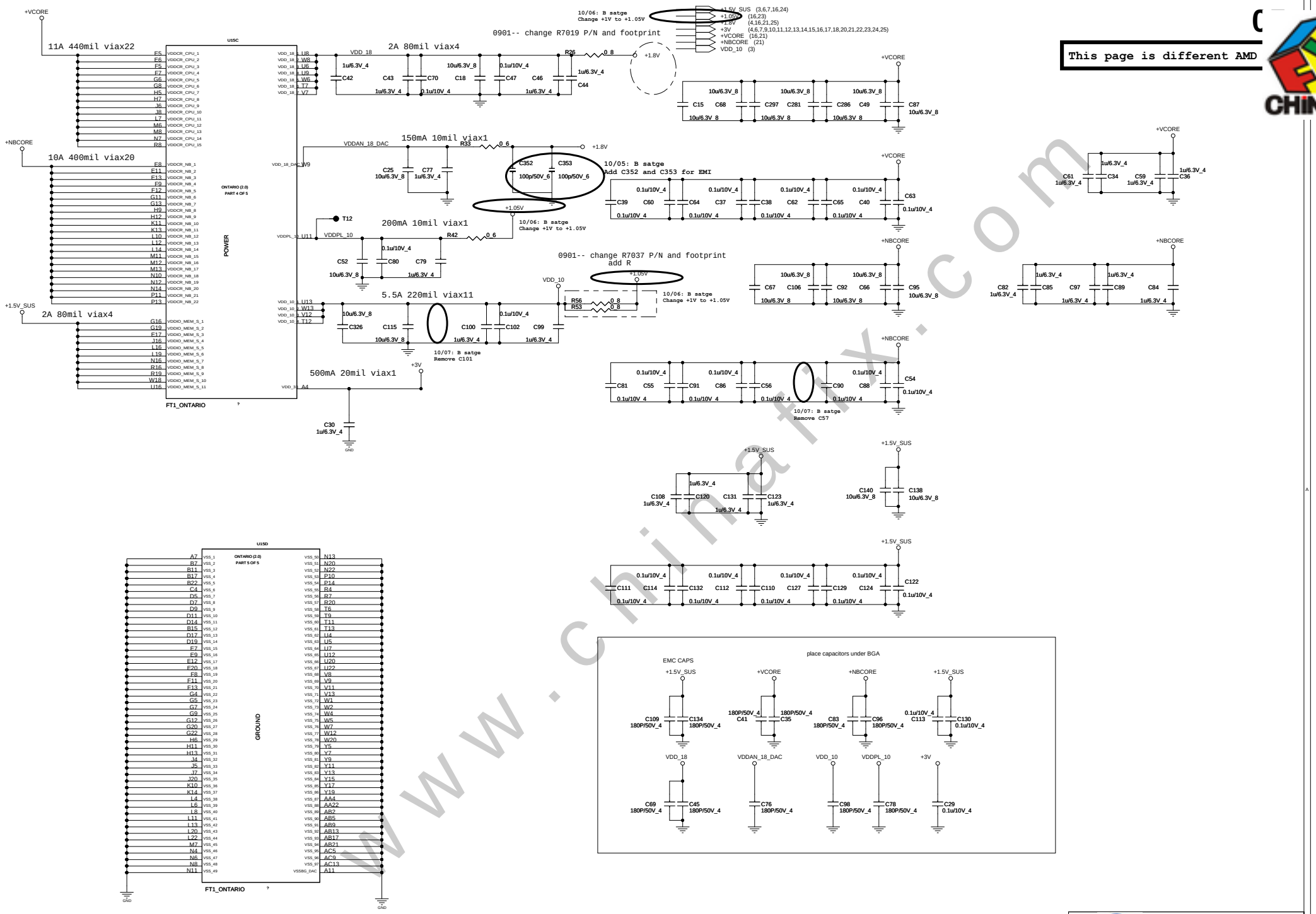

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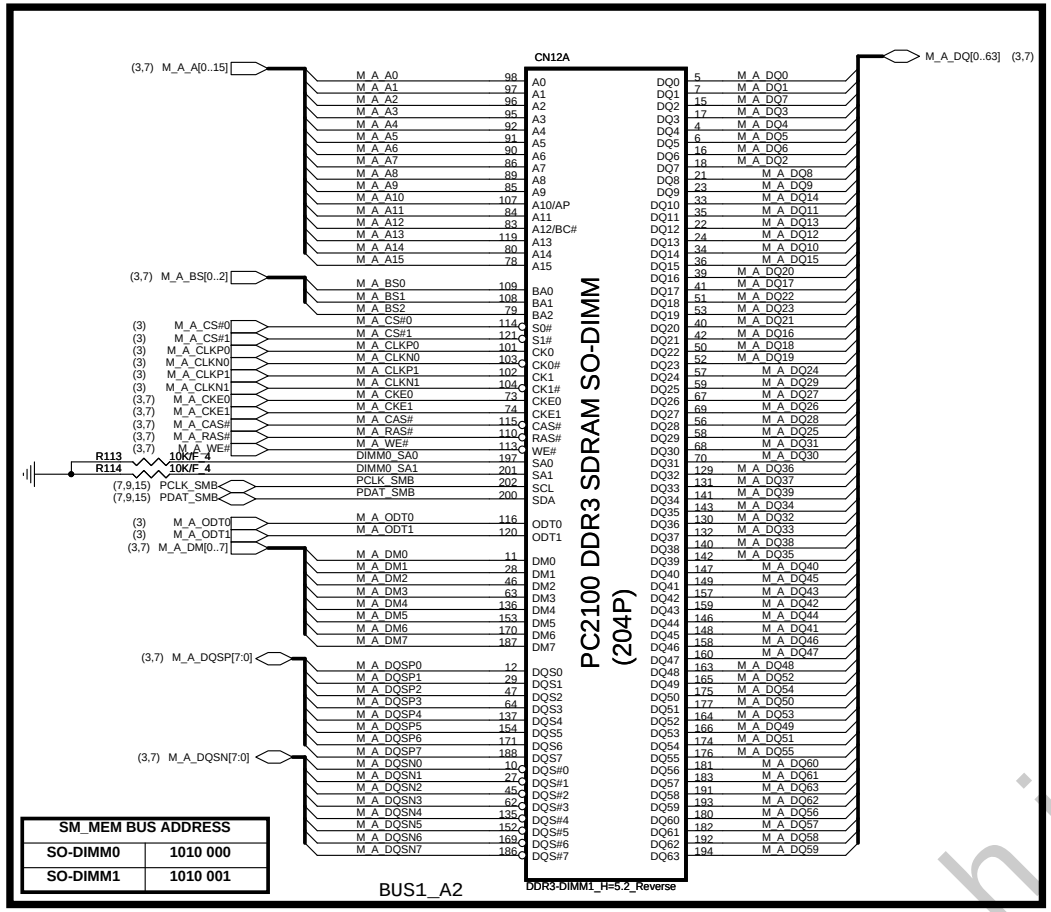
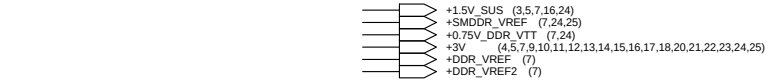
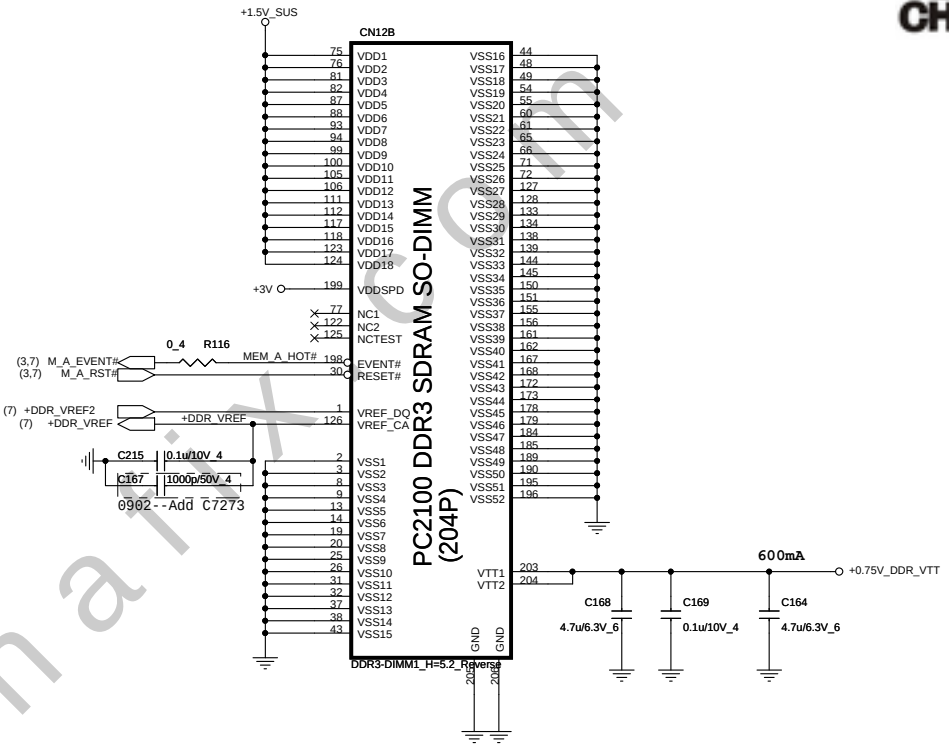
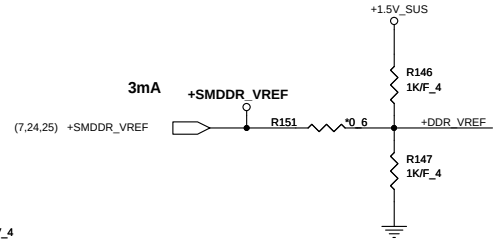
0830--P/N and footprint are follow ZR7B

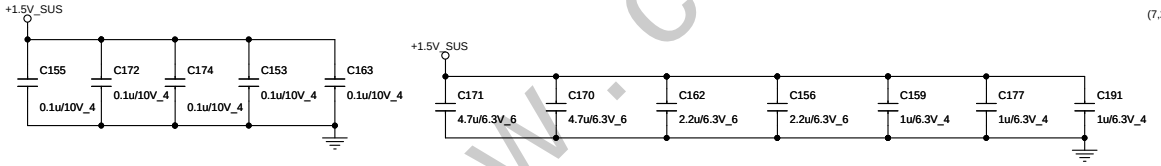


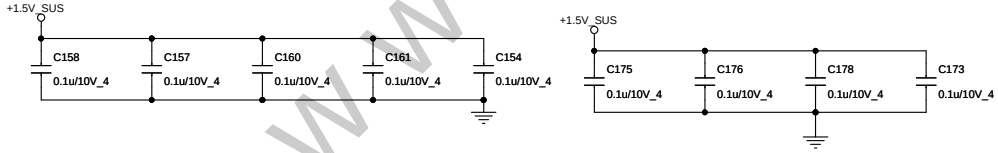
SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001











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	DDR3 SO-DIMM (RVS)	2A

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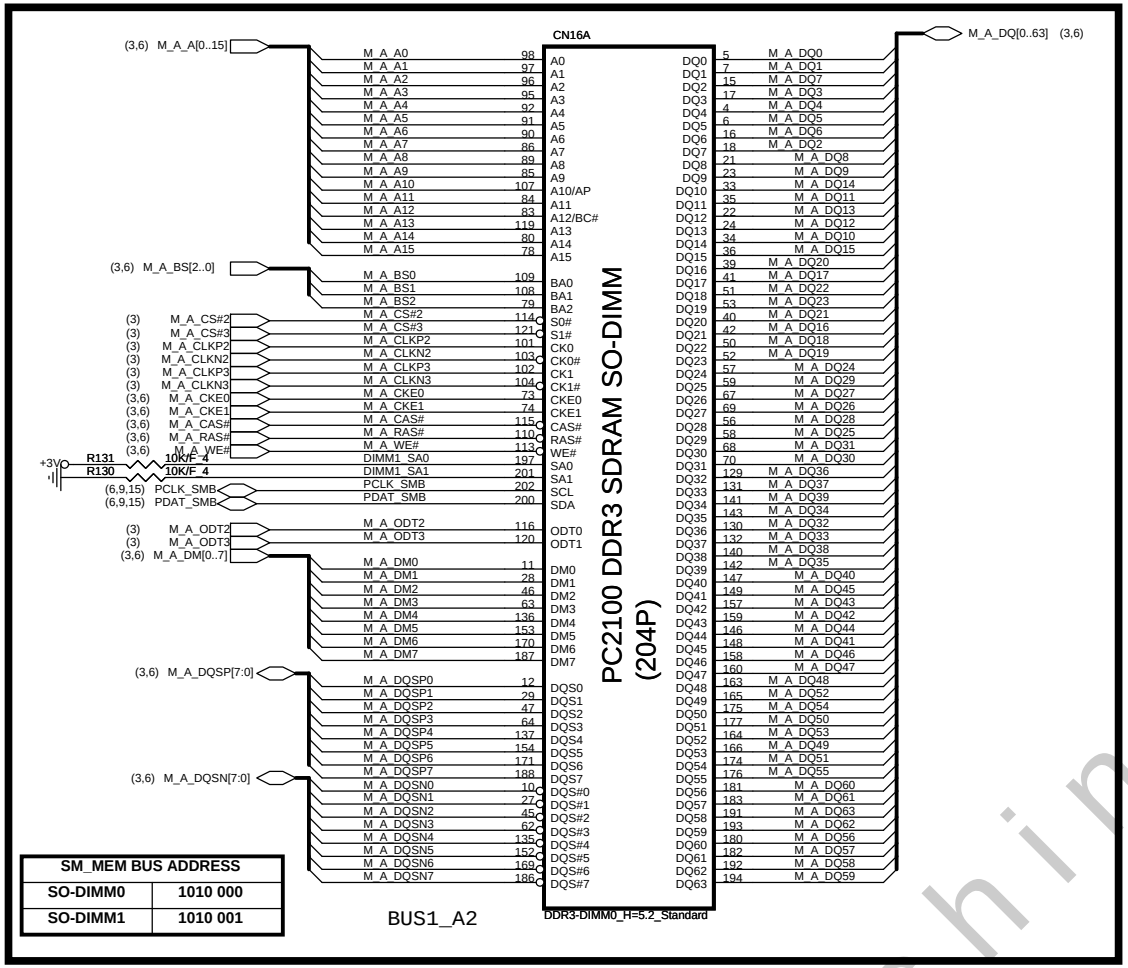
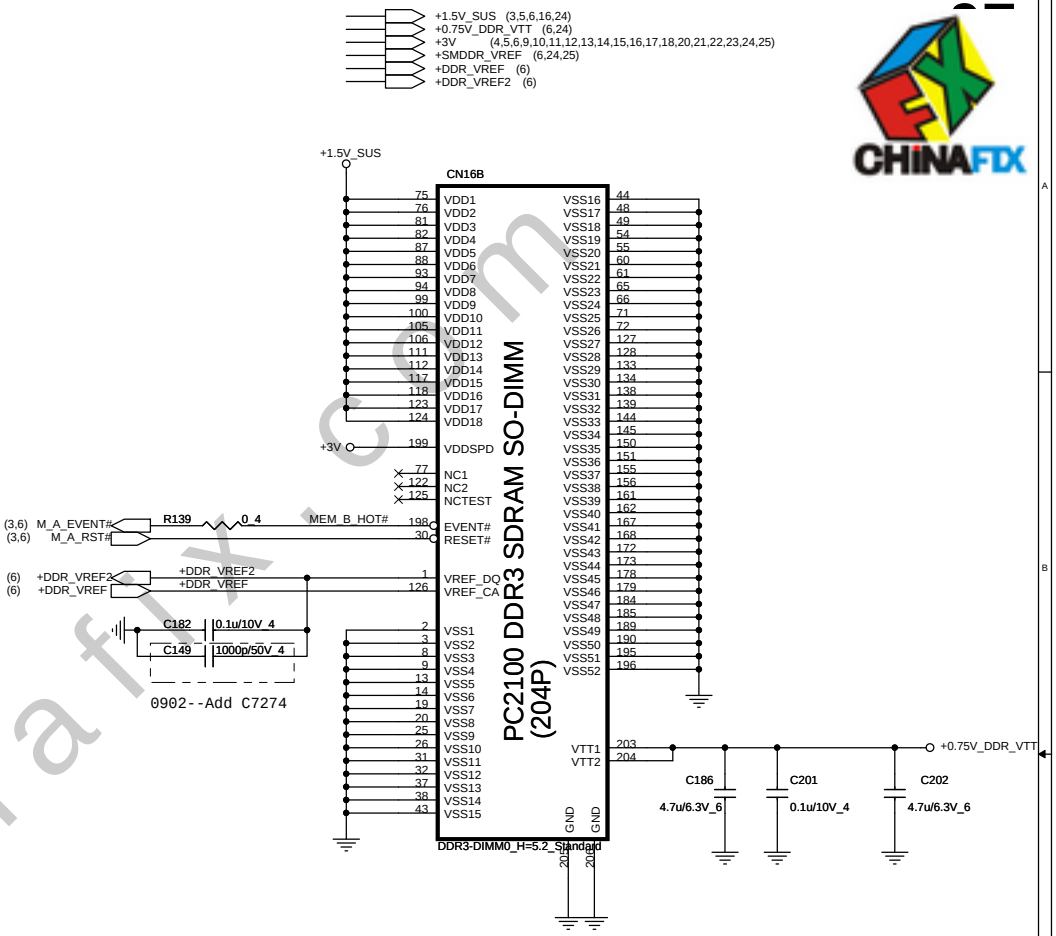
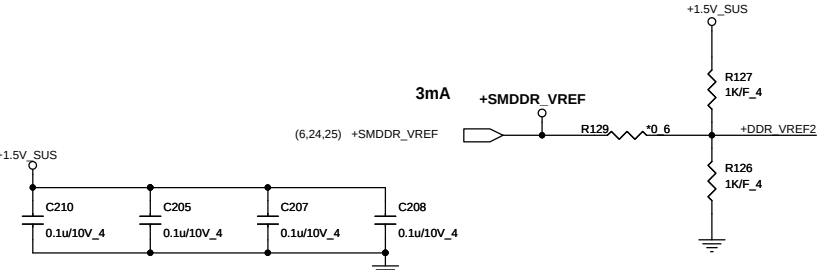
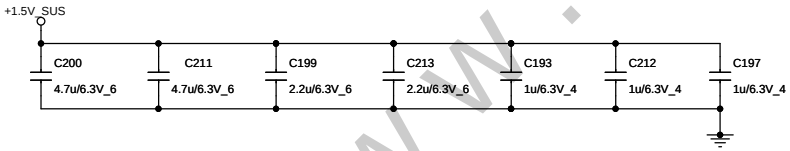
0830--P/N and footprint are follow ZR7B

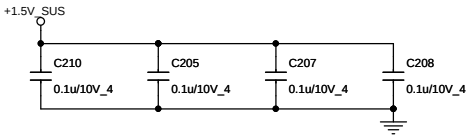


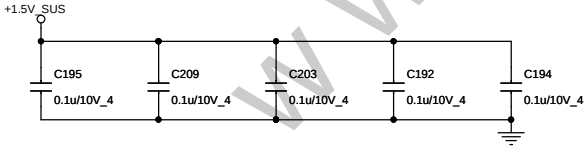
SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001

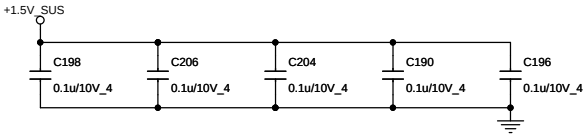












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	DDR3 SO-DIMM (STD)	2A

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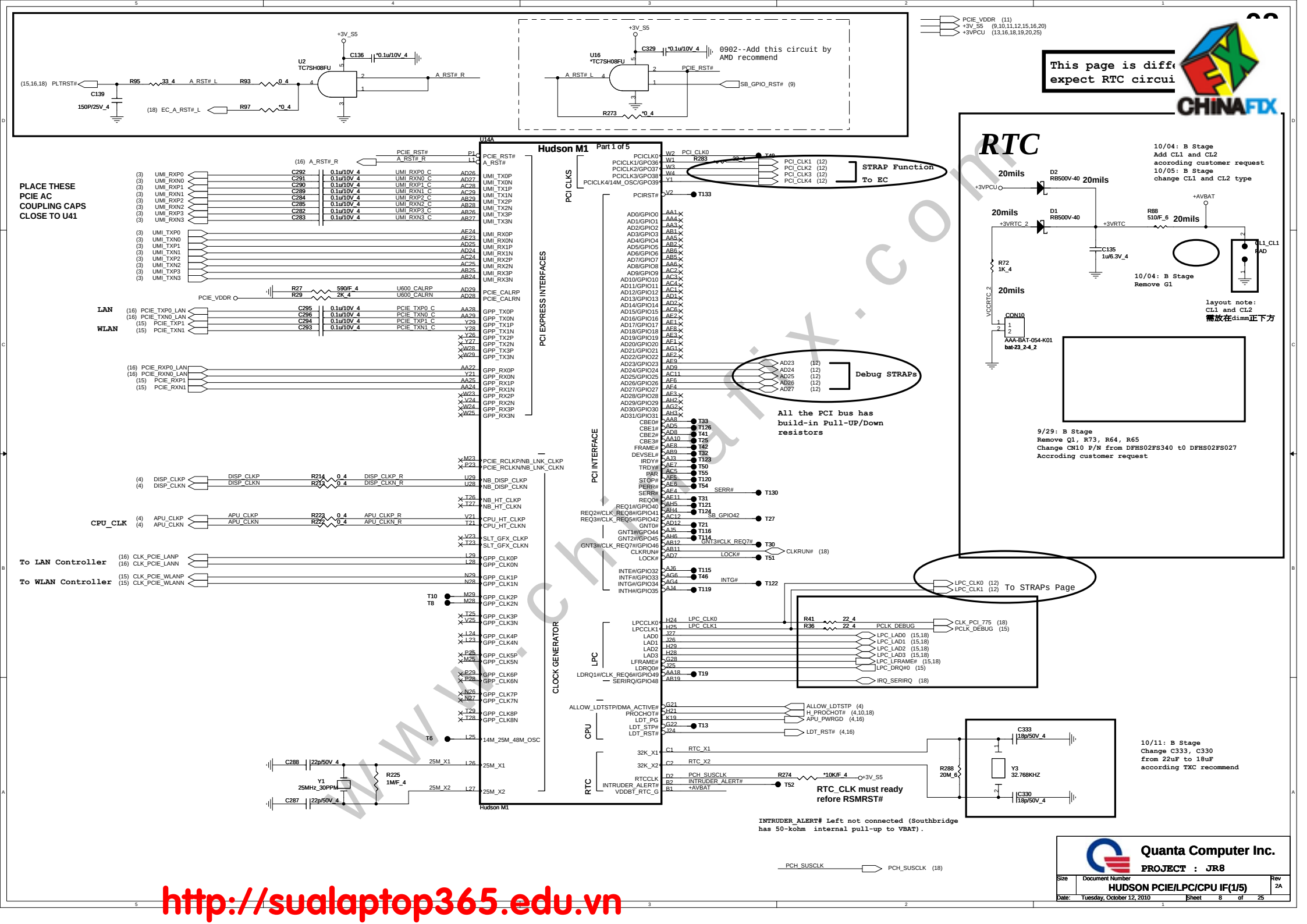

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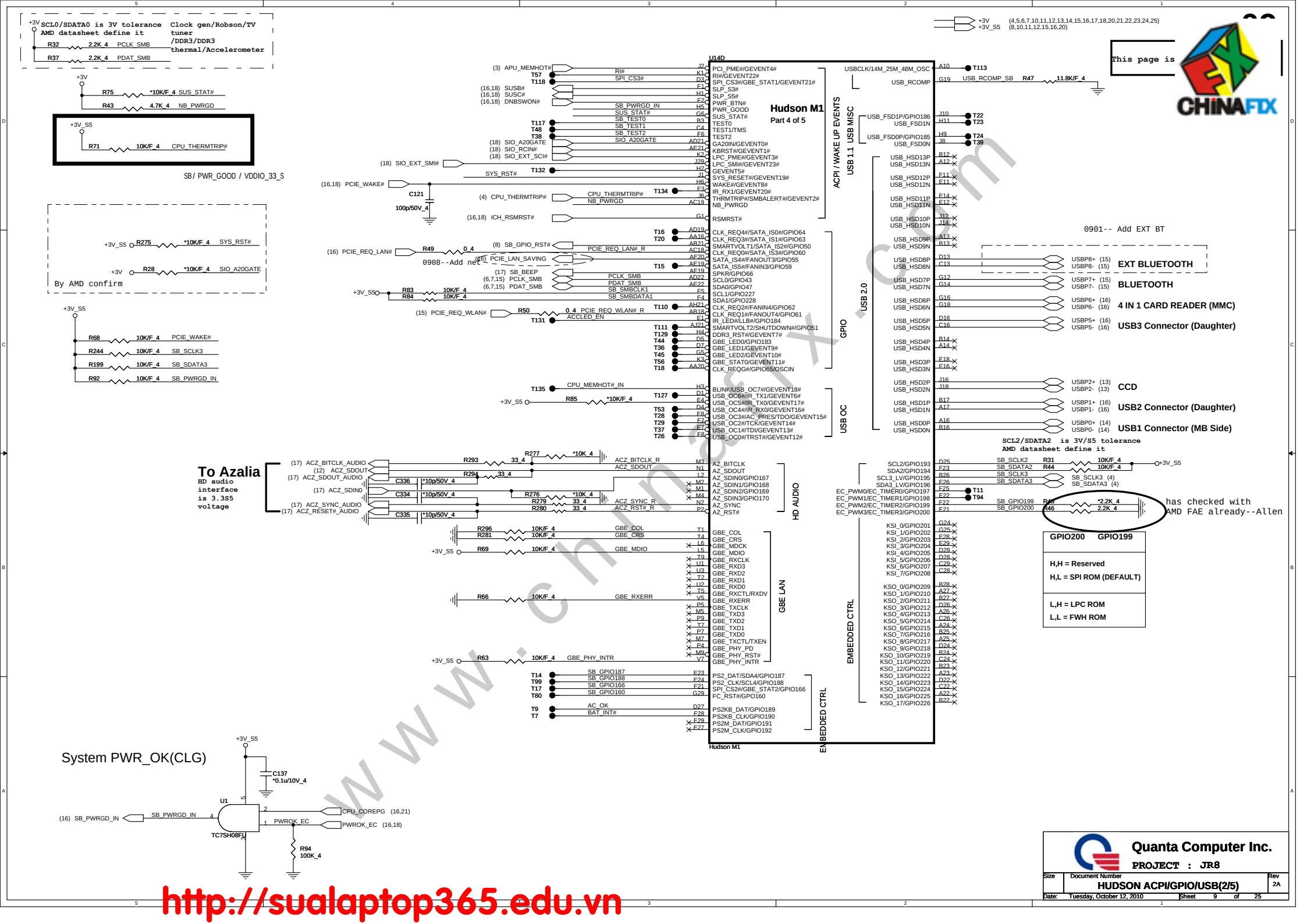
SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
Clock gen/Robson/TV tuner /DDR3/DDR3 thermal/Accelerometer
R32 2.2K_4 PCLK_SMB
R37 2.2K_4 PDAT_SMB
R75 *10K/F_4 SUS_STAT#
R43 4.7K_4 NB_PWRGD
R71 10K/F_4 CPU_THERMTRIP#
SB/ PWR_GOOD / VDDIO_33_S
R275 *10K/F_4 SYS_RST#
R28 *10K/F_4 SIO_A20GATE
By AMD confirm
R68 10K/F_4 PCIE_WAKE#
R244 10K/F_4 SB_SCLK3
R199 10K/F_4 SB_SDATA3
R92 10K/F_4 SB_PWRGD_IN
U14D
Hudson M1
Part 4 of 5
ACPI / WAKE UP EVENTS
USB 1.1 USB MISC
USB 2.0
GPIO
USB OC
HD AUDIO
GBE LAN
EMBEDDED CTRL
0908--Add net
0901-- Add EXT BT
EXT BLUETOOTH
BLUETOOTH
4 IN 1 CARD READER (MMC)
USB3 Connector (Daughter)
CCD
USB2 Connector (Daughter)
USB1 Connector (MB Side)
SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it
To Azalia
HD audio interface is 3.3S5 voltage
has checked with AMD FAE already--Allen
GPIO200 GPIO199
H,H = Reserved
H,L = SPI ROM (DEFAULT)
L,H = LPC ROM
L,L = FWH ROM
System PWR_OK(CLG)
U1
TC7SH08FU
C137 *0.1u/10V_4
R94 100K_4
SB_PWRGD_IN
CPU_COREPG (16,21)
PWROK_EC (16,18)
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HUDSON ACPI/GPIO/USB(2/5)
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SATA PORT 0,1,2,3 can support AHCI mode

PLACE SATA AC COUPLING CAPS CLOSE TO Hudson M1

AVDD_SATA (11)
+3V (4,5,6,7,9,11,12,13,14,15,16,17,18,20,21,22,23,24,25)
+3V_S5 (8,9,11,12,15,16,20)

This page is different AMD Nile

SATA HDD

(14) SATA_TXP0 — C328 .01U/16V/X7R_4 — SATA_TXP0_C — AH9 SATA_TX0P
(14) SATA_TXN0 — C327 .01U/16V/X7R_4 — SATA_TXN0_C — AJ9 SATA_TX0N
(14) SATA_RXN0 — AJ8 SATA_RX0N
(14) SATA_RXP0 — AH8 SATA_RX0P

U14B

Hudson M1
Part 2 of 5

SERIAL ATA

AH10 SATA_TX1P
AJ10 SATA_TX1N
AG10 SATA_RX1N
AF10 SATA_RX1P
AG12 SATA_TX2P
AF12 SATA_TX2N
AJ12 SATA_RX2N
AH12 SATA_RX2P
AH14 SATA_TX3P
AJ14 SATA_TX3N
AG14 SATA_RX3N
AF14 SATA_RX3P
AG17 SATA_TX4P
AF17 SATA_TX4N
AJ17 SATA_RX4N
AH17 SATA_RX4P
AJ18 SATA_TX5P
AH18 SATA_TX5N
AH19 SATA_RX5N
AJ19 SATA_RX5P

PLACE SATA_CAL RES VERY CLOSE TO BALL OF Hudson M1

XTLVDD_SATA-- SATA crystal power

PLVDD_SATA-- SATA PLL POWER

AVDD_SATA — R54 1K/F_4 — R51 931/F_4 — SATA_CALRP — SATA_CALRN — AB14 SATA_CALRP — AA14 SATA_CALRN

(16) SATA_LED# — AD11 SATA_ACT#/GPIO67

C314 *22p/50V_4 — SATA_X1 — AD16 SATA_X1
Y2 *25MHz_30PPM — R255 *1M/F_4
C319 *22p/50V_4 — SATA_X2 — AC16 SATA_X2

SPI ROM

T43 SPI_DI — J5 SPI_DI/GPIO164
T47 SPI_DO — E2 SPI_DO/GPIO163
T58 SPI_CLK — K4 SPI_CLK/GPIO162
T34 SPI_CS1# — K9 SPI_CS1#/GPIO165
T125 ROM_RST# — G2 ROM_RST#/GPIO161

Hudson M1

FLASH

FC_CLK — AH28 — T89
FC_FBCLKOUT — AG28 — T84
FC_FBCLKIN — AF26 — T88
FC_OE#/GPIO145 — AF28 — T82
FC_AVD#/GPIO146 — AG29 — T87
FC_WE#/GPIO148 — AG25
FC_CE1#/GPIO149 — AF27
FC_CE2#/GPIO150 — AE29 — T81
FC_INT1/GPIO144 — AF29 — T83
FC_INT2/GPIO147 — AH27 — T90
FC_ADQ0/GPIO128 — AJ27 — T95
FC_ADQ1/GPIO129 — AJ26 — T97
FC_ADQ2/GPIO130 — AH25 — T98
FC_ADQ3/GPIO131 — AH24 — T102
FC_ADQ4/GPIO132 — AG23 — T104
FC_ADQ5/GPIO133 — AH23 — T105
FC_ADQ6/GPIO134 — AJ22 — T108
FC_ADQ7/GPIO135 — AG21 — T112
FC_ADQ8/GPIO136 — AF21 — T109
FC_ADQ9/GPIO137 — AH22 — T107
FC_ADQ10/GPIO138 — AJ23 — T106
FC_ADQ11/GPIO139 — AF23 — T101
FC_ADQ12/GPIO140 — AJ24 — T103
FC_ADQ13/GPIO141 — AJ25 — T100
FC_ADQ14/GPIO142 — AG25
FC_ADQ15/GPIO143 — AH26 — T96

HW MONITOR

FANOUT0/GPIO52 — W5 — BOARD_ID0
FANOUT1/GPIO53 — W6 — BOARD_ID1
FANOUT2/GPIO54 — Y9 — SB_PROCHOT#
FANIN0/GPIO56 — W7 — BOARD_ID2
FANIN1/GPIO57 — V9 — BOARD_ID3
FANIN2/GPIO58 — W8 — BOARD_ID4
TEMPIN0/GPIO171 — R6 — TEMPIN0
TEMPIN1/GPIO172 — A6 — TEMPIN1
TEMPIN2/GPIO173 — A5 — TEMPIN2
TEMPIN3/TALERT#/GPIO174 — R5 — SB_TALERT# — SB_TALERT# (4)
TEMP_COMM — C7
VIN0/GPIO175 — A3 — CPU_TYPE
VIN1/GPIO176 — B4 — SB_HOLE_TIME
VIN2/GPIO177 — A4 — CPU_SENSOR
VIN3/GPIO178 — C5 — VIN2 — R267 10K_4
VIN4/GPIO179 — A7 — VIN3 — R262 10K_4
VIN5/GPIO180 — B7 — VIN4 — R261 10K_4
VIN6/GBE_STAT3/GPIO181 — B8 — VIN5 — R258 10K_4
VIN7/GBE_LED3/GPIO182 — A8 — BOARD_ID5

NC1 — G27
NC2 — Y2

(4,8,18) H_PROCHOT# — H_PROCHOT# — D3 RB500V-40 — SB_PROCHOT#

0831--modify location

0831--add circuit

AMD recommand : TEMPIN0 / TEMPIN1 / TEMPIN2 can not maintain on floating stages when without usage. Do not care pull high or pull down.

TEMPIN2
TEMPIN1
TEMPIN0
R266 10K_4
R265 10K_4
R268 10K_4

MB ID

CPU THERMAL	GPIO52
External	1
SB-TSI	0

	GPIO57
	1
	0

SB8XX Hold Time	GPIO53
1.2V	1
1.1V	0

	GPIO58
	1
	0

DU1/MK2	GPIO56
MK2.0 AMD	1
DU1.0 AMD	0

	GPIO182
	1
	0

+3V

GPIO52
R80 10K_4 BOARD_ID0 R91 *10K_4

GPIO53
R79 10K_4 BOARD_ID1 R90 *10K_4

GPIO56
R78 10K_4 BOARD_ID2 R89 *10K_4

GPIO57
R61 10K_4 BOARD_ID3 R60 *10K_4

GPIO58
R282 10K_4 BOARD_ID4 R297 *10K_4

+3V_S5

GPIO182
R59 10K_4 BOARD_ID5 R259 *10K_4
R77 *10K/F_4 CPU_TYPE R86 10K/F_4
R70 *10K/F_4 CPU_SENSOR R67 10K/F_4
R270 *10K/F_4 SB_HOLE_TIME R271 10K/F_4

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	HUDSON SATA/BIDs(3/5)	2A

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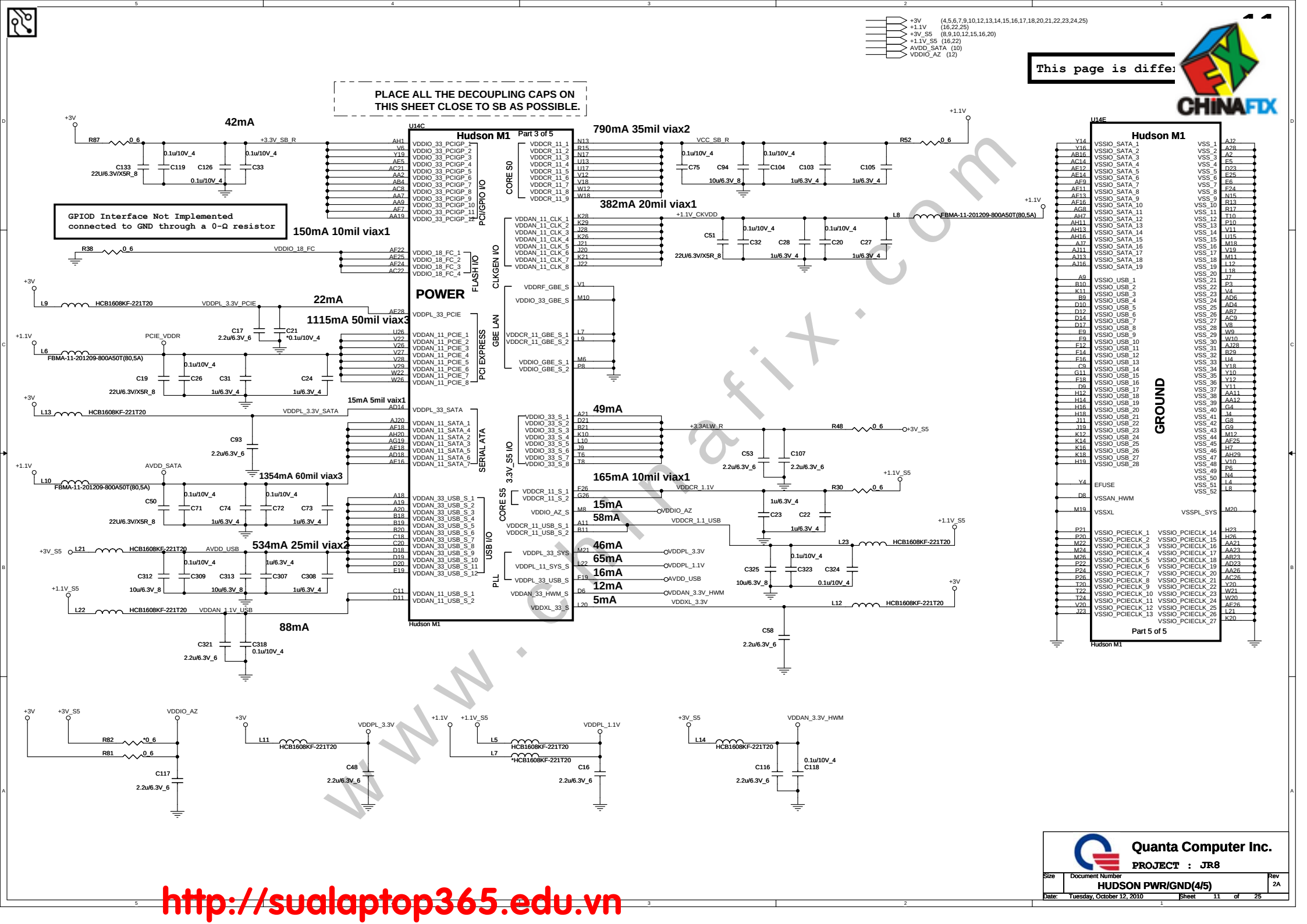

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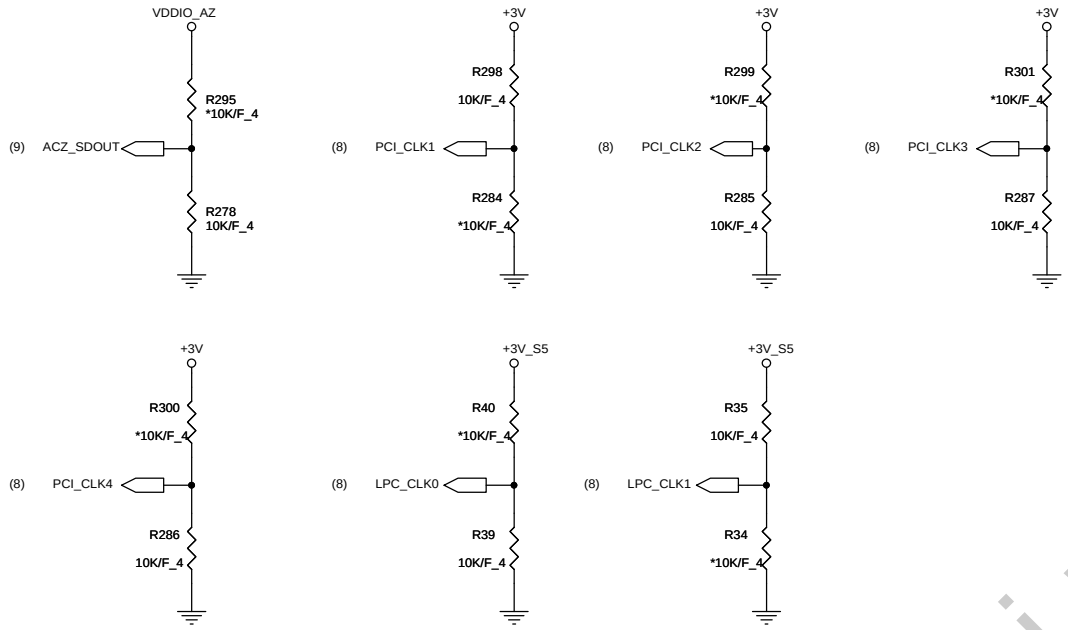
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

intermal have pull
Hi 10K , confirm AMD
ward this pull Hi
not need

VDDIO_AZ (11)
+3V (4,5,6,7,9,10,11,13,14,15,16,17,18,20,21,22,23,24,25)
+3V_S5 (8,9,10,11,15,16,20)

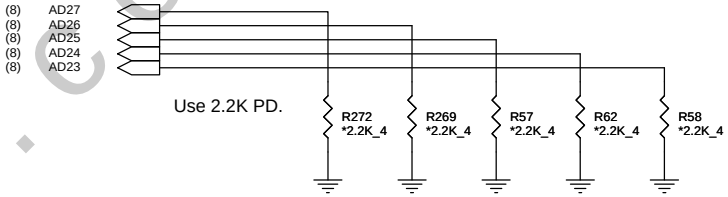
REQUIRED STRAPS



PCI_CLK4 CPU/NB HT Clock Selection
0 V - Reserved.
3.3 V - Required setting for integrated clock mode.
This strap is not used if the strap CLKGEN is
configured for external clock generator mode.

DEBUG STRAPS

HUDSON-M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

REQUIRED STRAPS

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM (Default)
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM L,L = FWH ROM

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Size	Document Number	Rev
	HUDSON STRAPS/PWRGD(5/5)	2A

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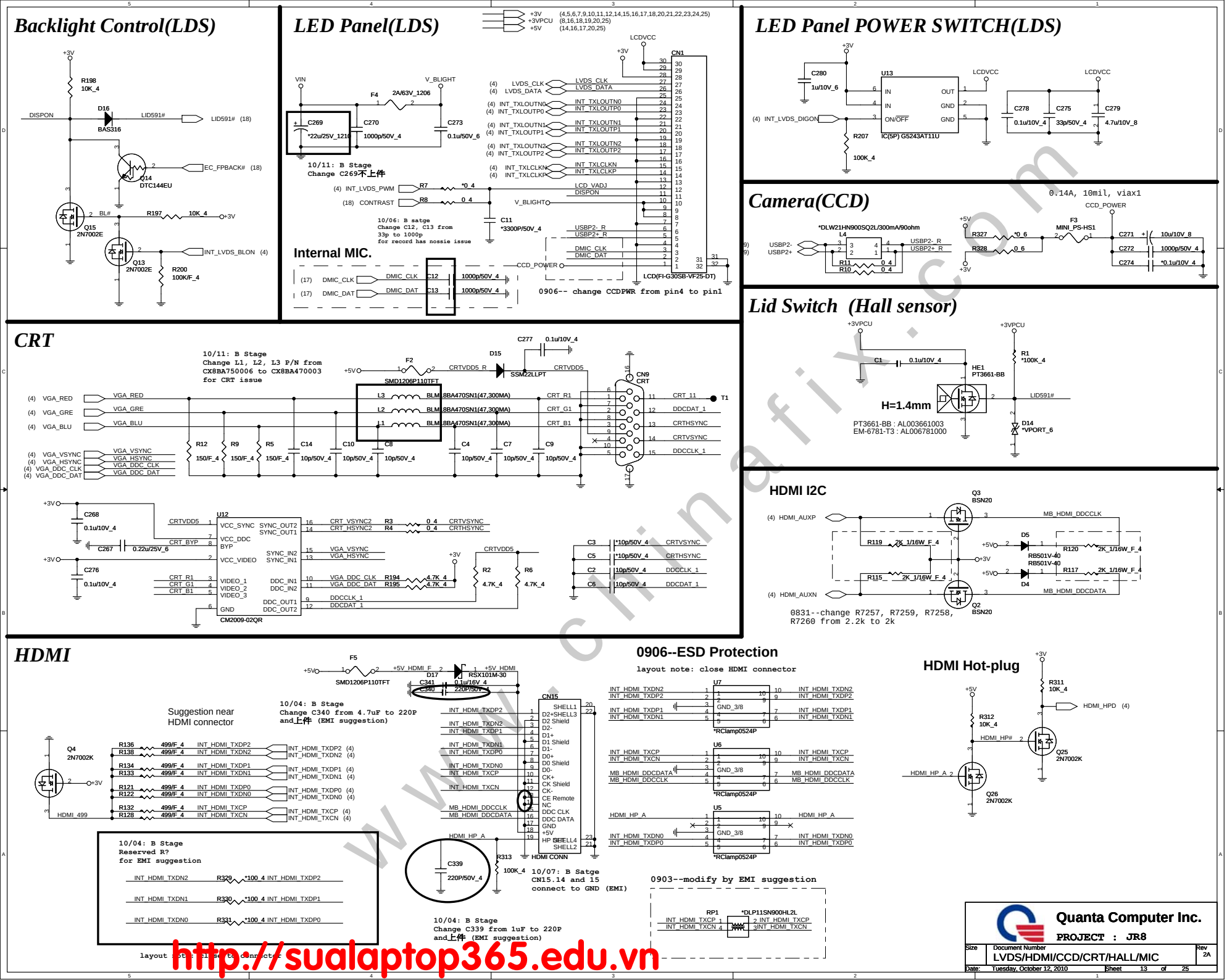

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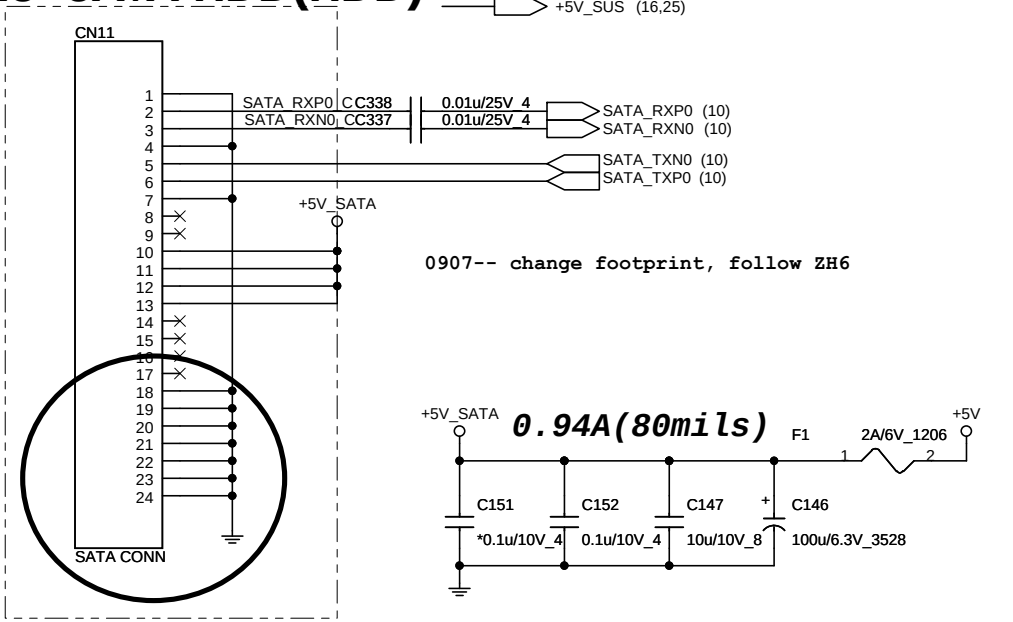
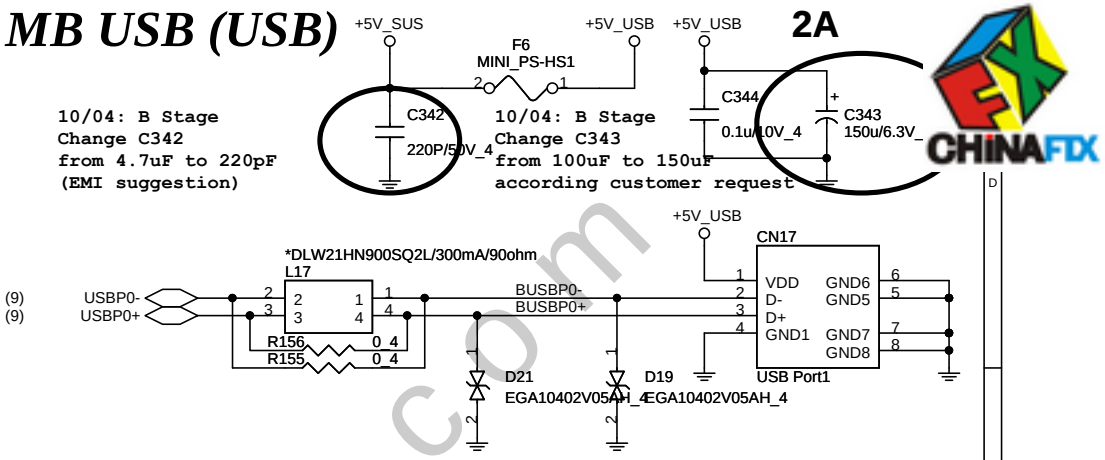
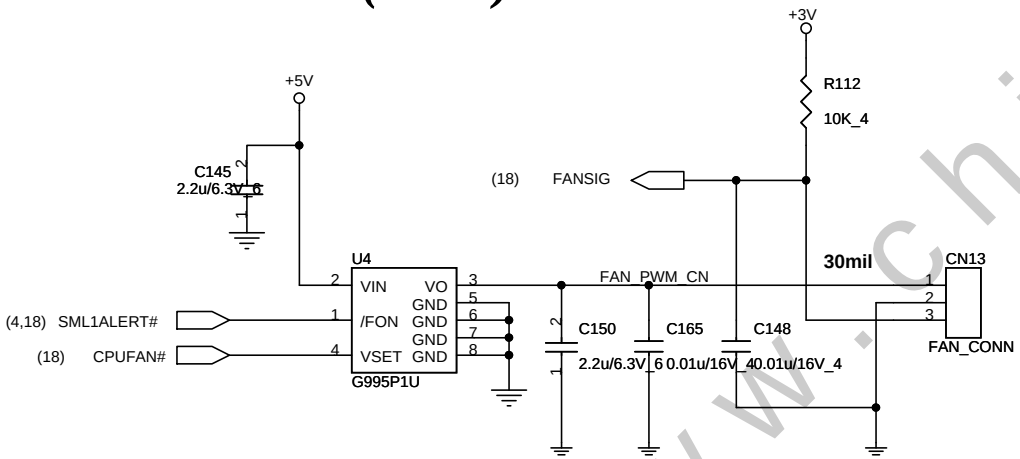
2.5" SATA HDD(HDD)



MB USB (USB)

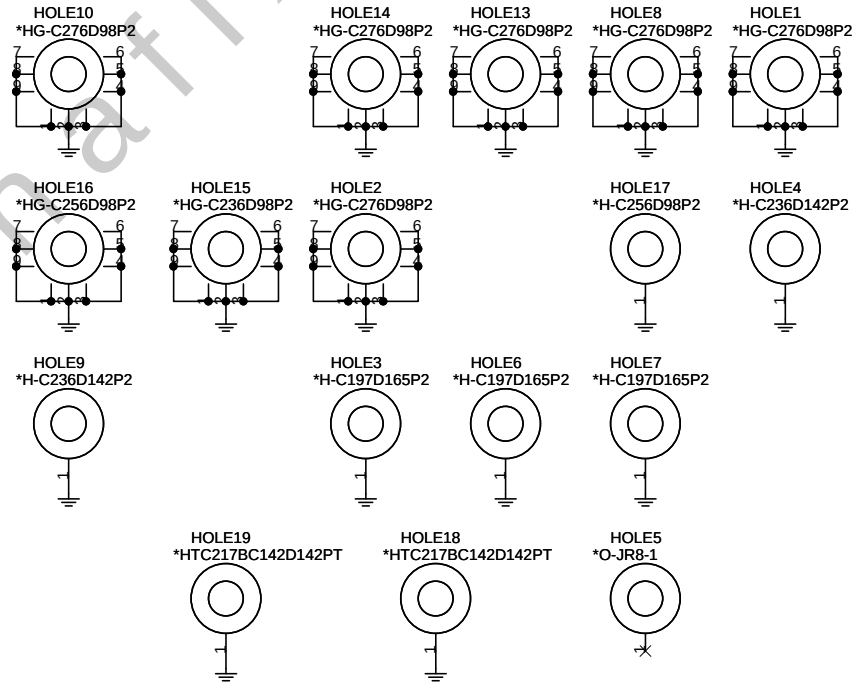


CPU FAN CTRL(THM)



0903--Modify circuit...follow ZQ9

HOLE



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PROJECT : JR8		
Size	Document Number: HDD/USB/FAN/HOLE	Rev 2A
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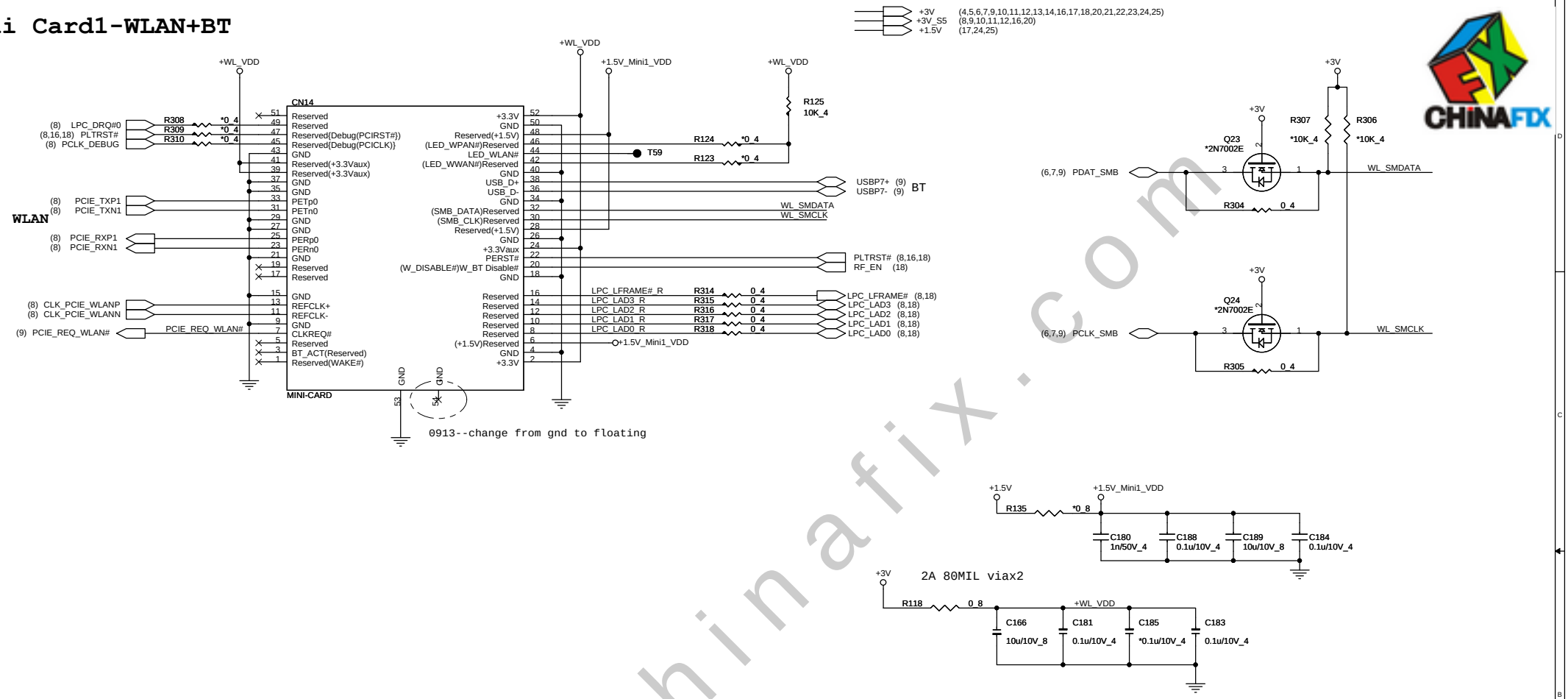
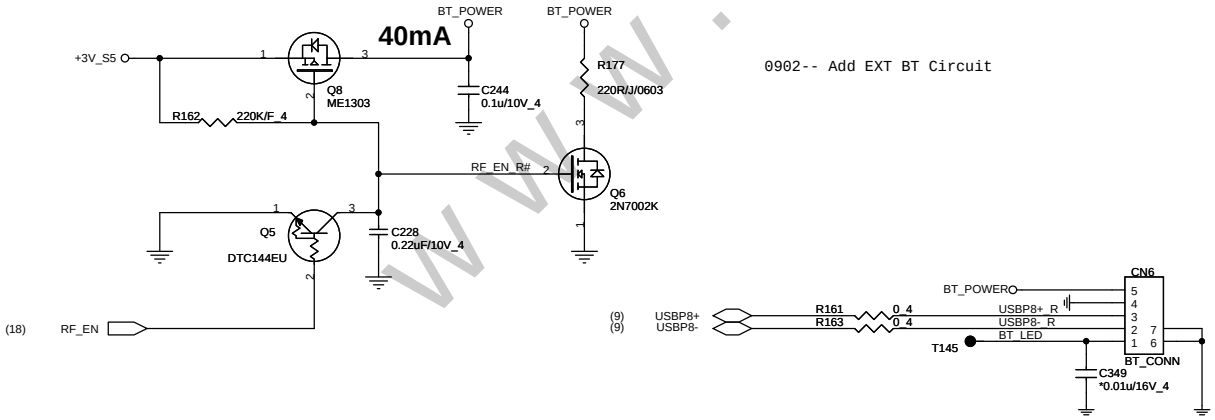
Mini Card1-WLAN+BT



EXT BT



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PROJECT : JR8

Size	Document Number	Rev
	MINE PCIE / EXT BT	2A

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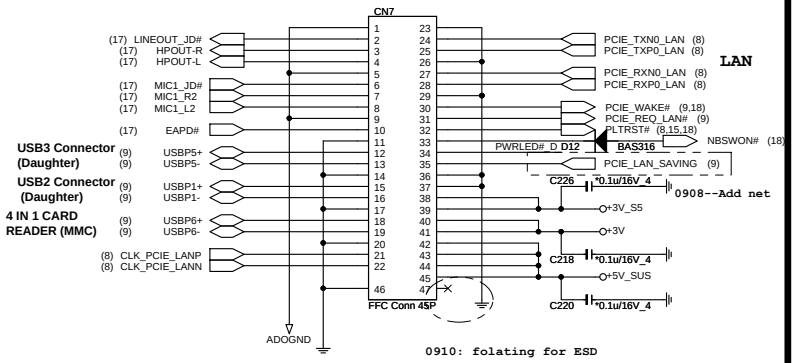
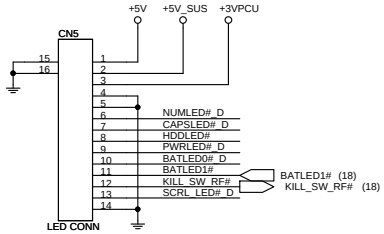
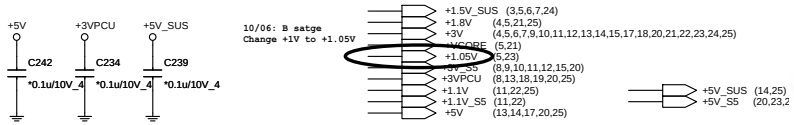
Card Reader/USB DB CONNECTER(MMC)/Power Connector

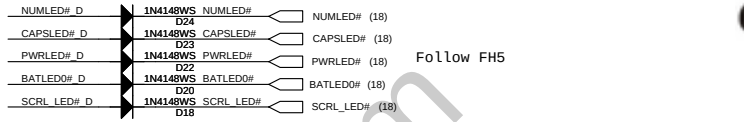


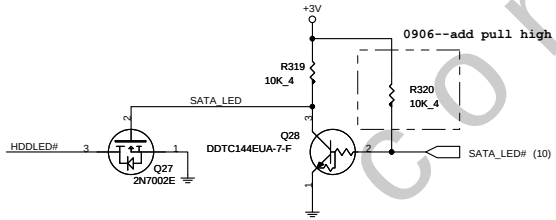
0910: folating for ESD

LED D/B (UIF)





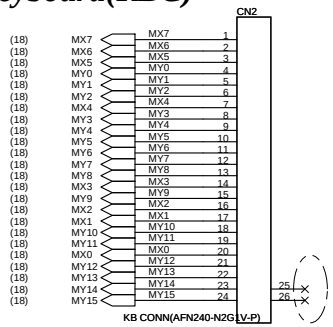




Close LED Conn.

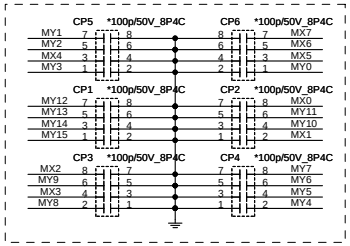
NUMLED# D	C350	*220P/50V_4
CAPSLED# D	C348	*220P/50V_4
HDDLED#	C231	*220P/50V_4
PWRLED# D	C347	*220P/50V_4
BATLED0# D	C346	*220P/50V_4
BATLED1#	C227	*220P/50V_4
KILL_SW_RF#	C224	*220P/50V_4
SCRL_LED# D	C345	*220P/50V_4

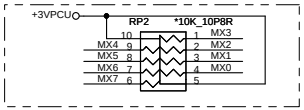
Keyboard(KBC)



0913--change from gnd to floating

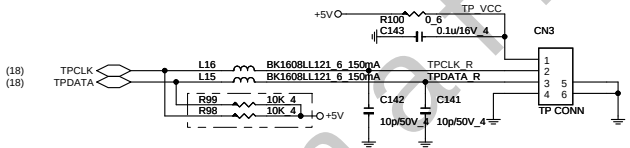
For EMI Reserve Caps for debug





0901--EC vender recommend reserved

TP Connector

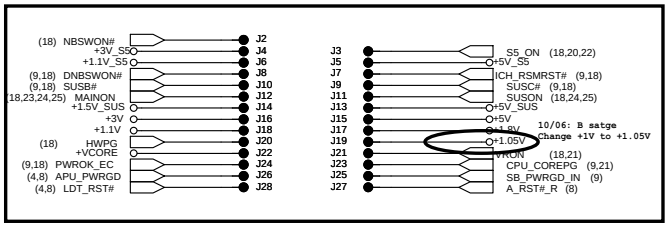


0901--EC vender recommend using 10K

Power Sequence

0903--Add CN18 Connecotr

10/07: B Satge
Remove CN18 and
Add J2~J28 test point



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PROJECT : JR8

Size	Document Number	Rev
	KB/LED/TP/DB	2A

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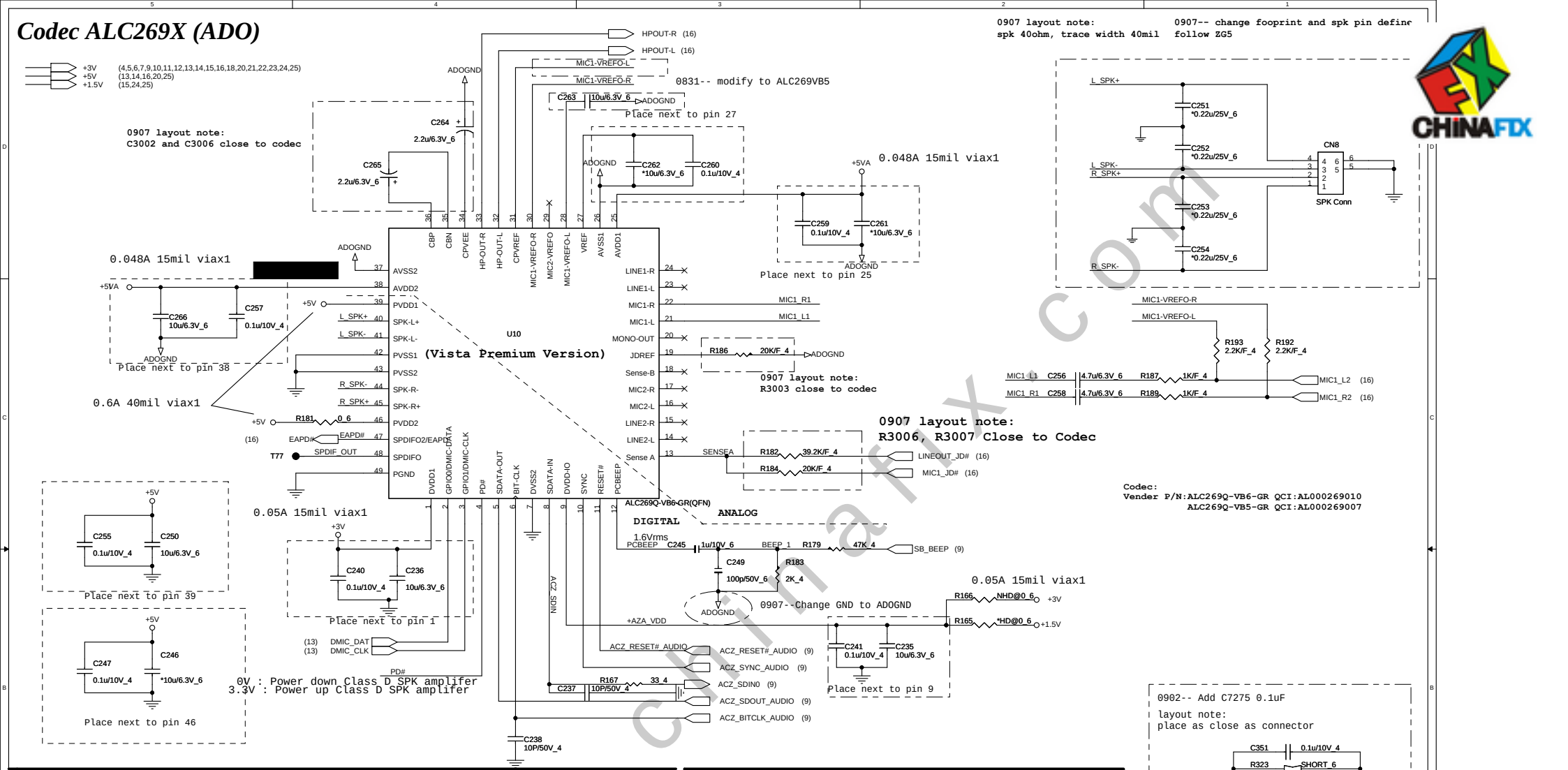
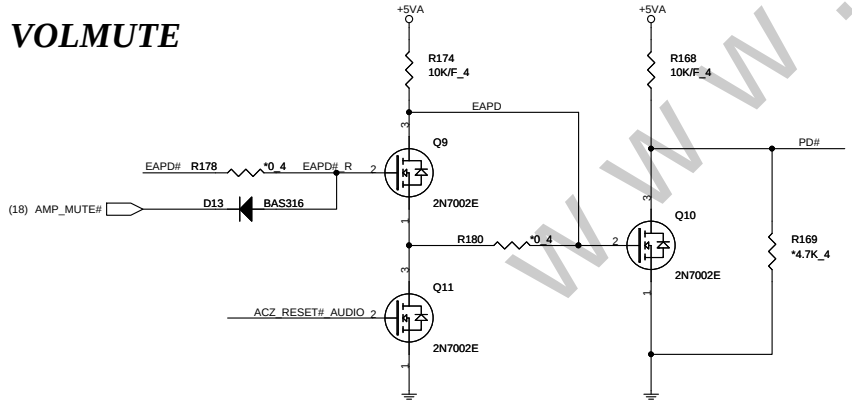
Codec ALC269X (ADO)



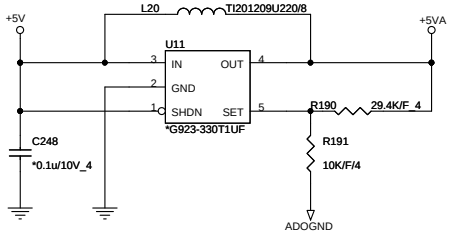
VOLMUTE



Power (ADO)

0907--L3000上件, U3001不上件
--by vender suggestion

Demodulation Filter
Place close to Codec



Quanta Computer Inc.

PROJECT : JR8

Size	Document Number	Rev
	Audo Codec (ALC2690)	2A

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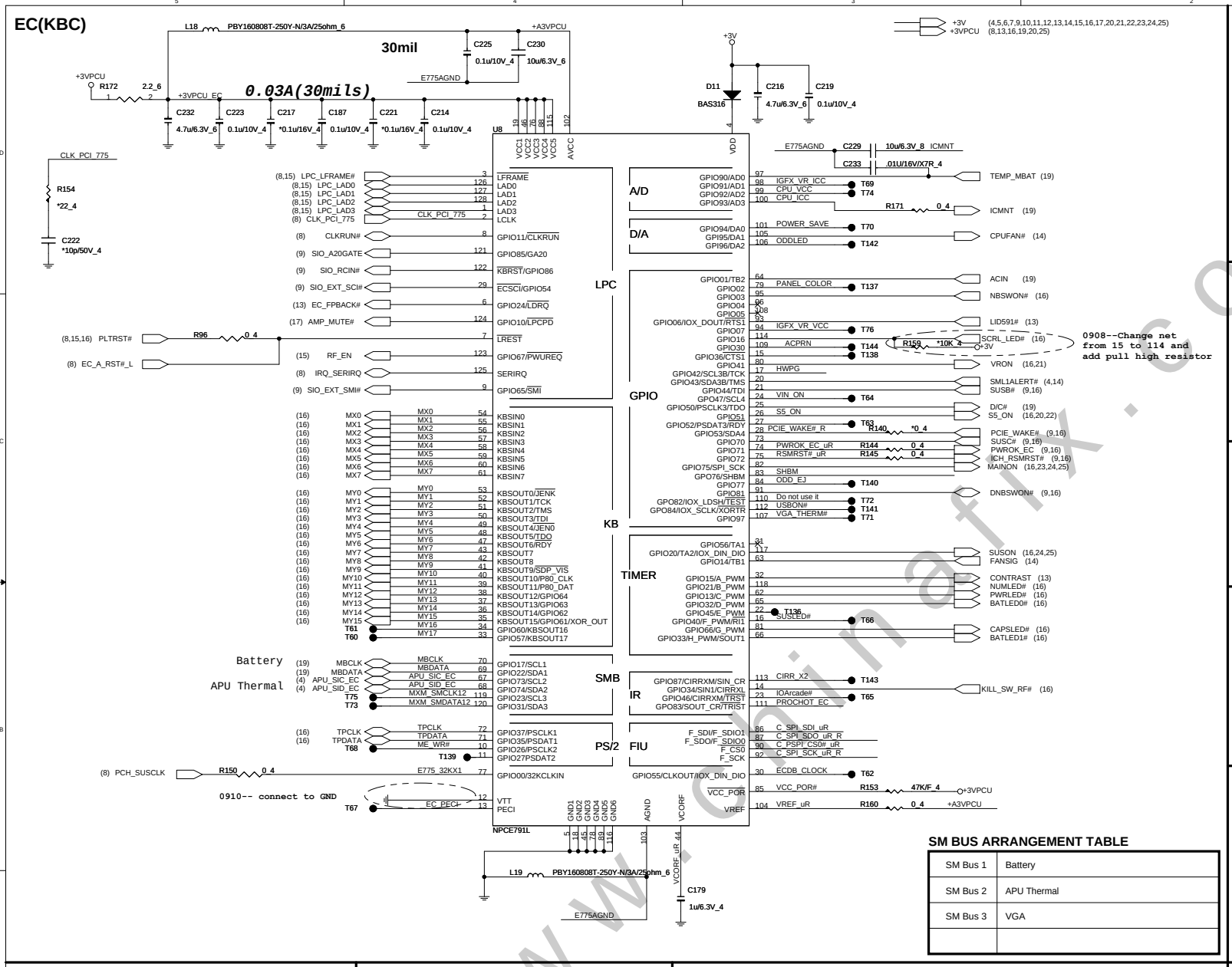
EC(KBC)



SM BUS ARRANGEMENT TABLE

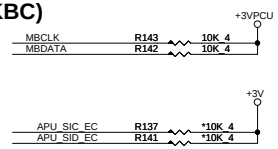
SM Bus 1	Battery
SM Bus 2	APU Thermal
SM Bus 3	VGA

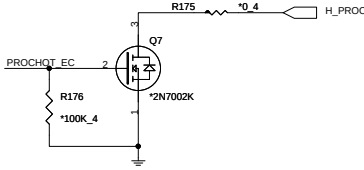
I/O ADDRESS SETTING(KBC)

SHBM — SHBM — R152 10K_4

Disable (non share SPI ROM) : no external PU resistor
enable (share SPI ROM) : 10Kohm external PD resistor

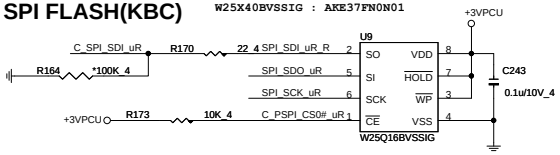
SM BUS PU(KBC)





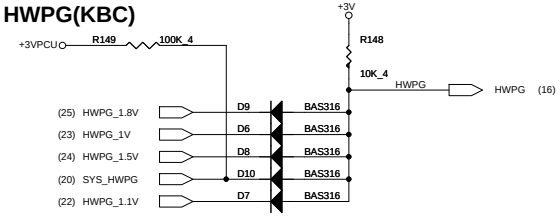
SPI FLASH(KBC)

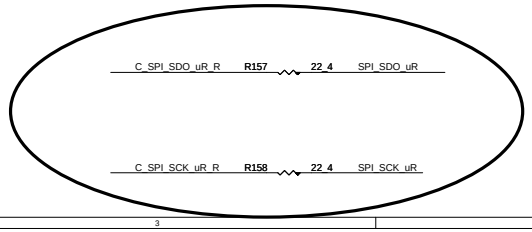
socket : DG008000031
W25X40BVSSIG : AKE37FN0N01



1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by
default, the flash device should be 50MHz (or faster)

HWPG(KBC)





Quanta Computer Inc.
PROJECT : JR8

Size	Document Number	Rev
	WPCE791 & FLASH	2A

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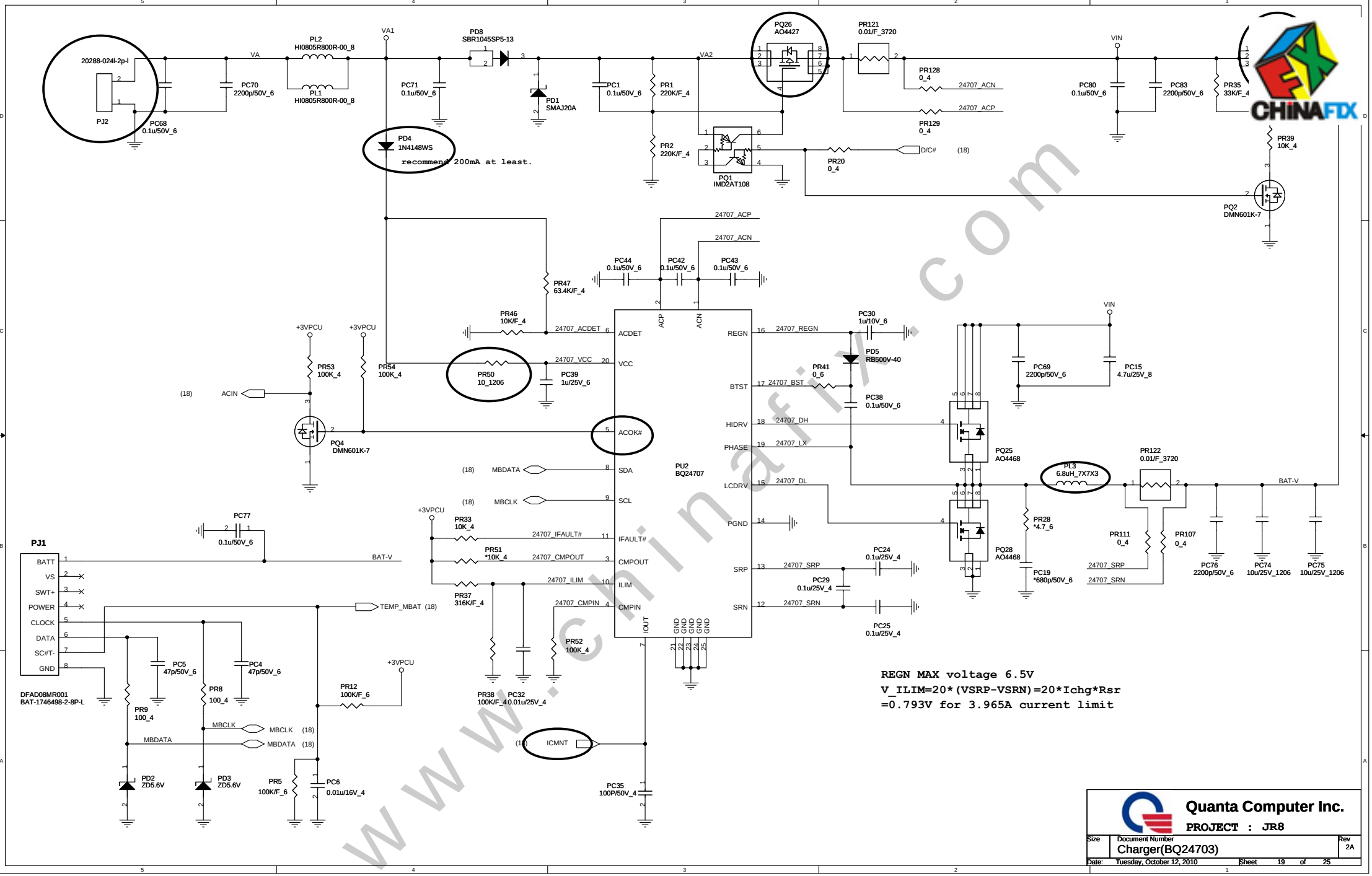

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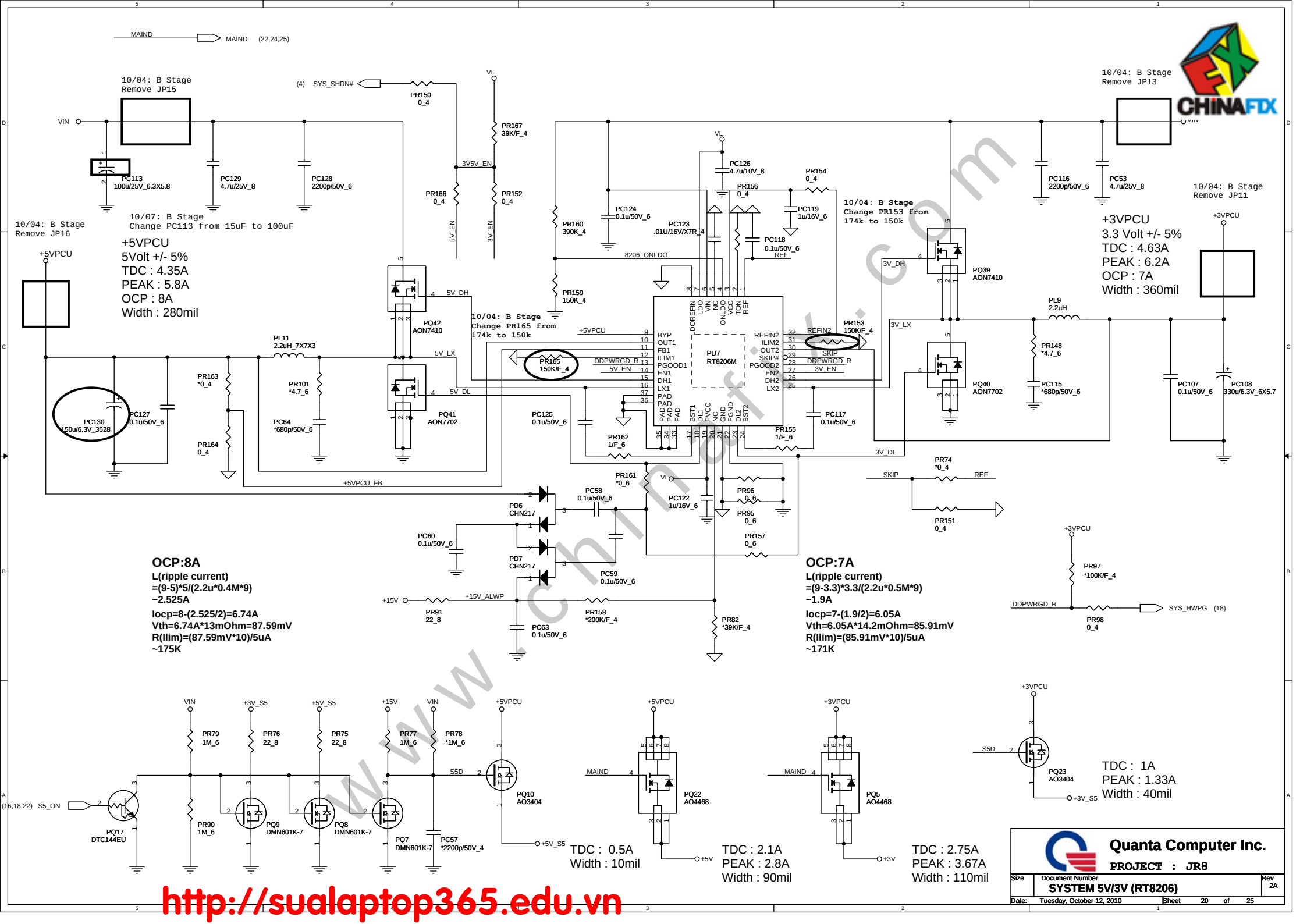

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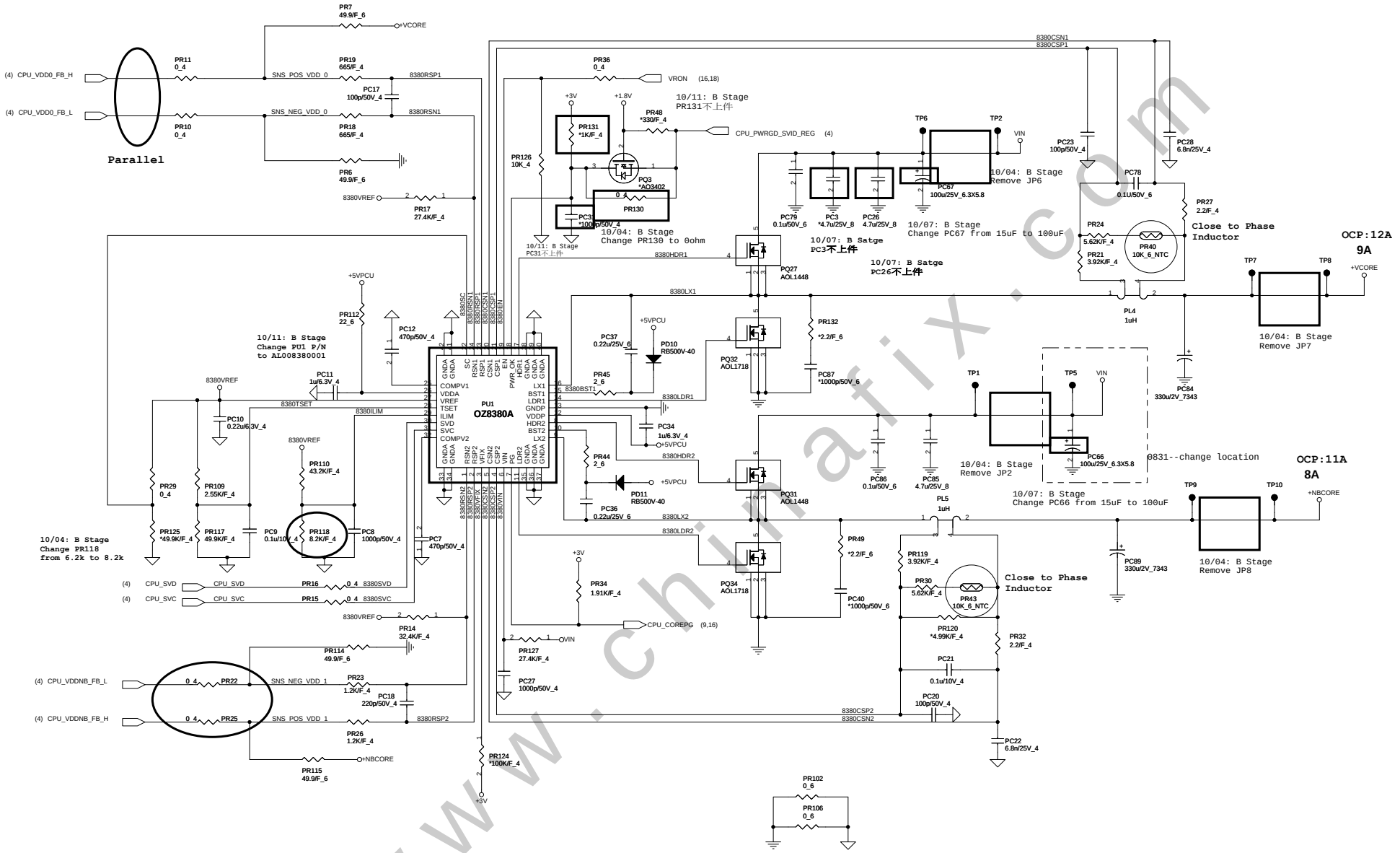

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PROJECT : JR8

Size	Document Number	Rev
	CPU Core (OZ8380)	2A

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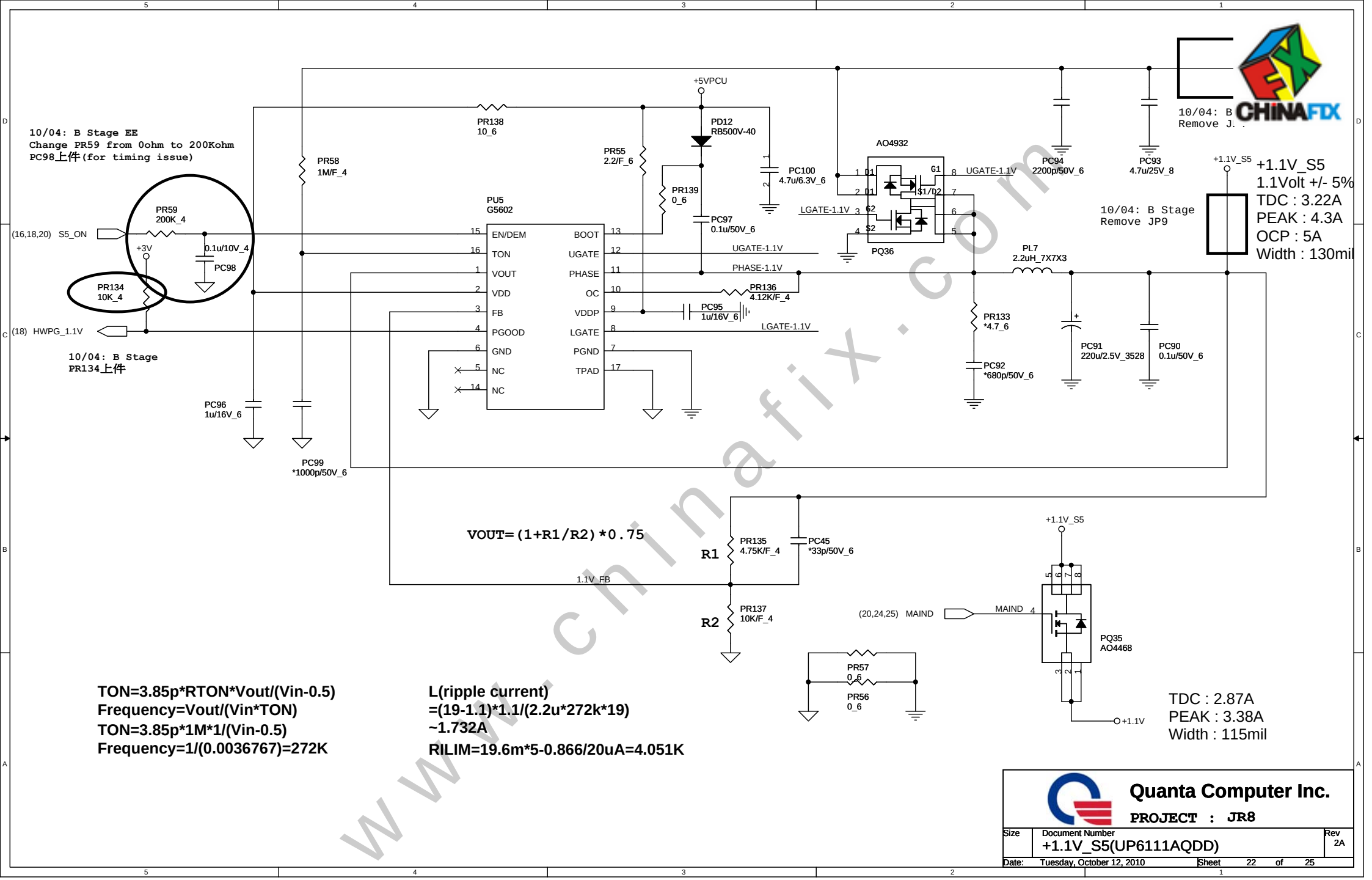

TON=3.85p*RTON*Vout/(Vin-0.5)
Frequency=Vout/(Vin*TON)
TON=3.85p*1M*1/(Vin-0.5)
Frequency=1/(0.0036767)=272K

L(ripple current)
=(19-1.1)*1.1/(2.2u*272k*19)
~1.732A
RILIM=19.6m*5-0.866/20uA=4.051K

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PROJECT : JR8

Size	Document Number	Rev
	+1.1V_S5(UP6111AQDD)	2A

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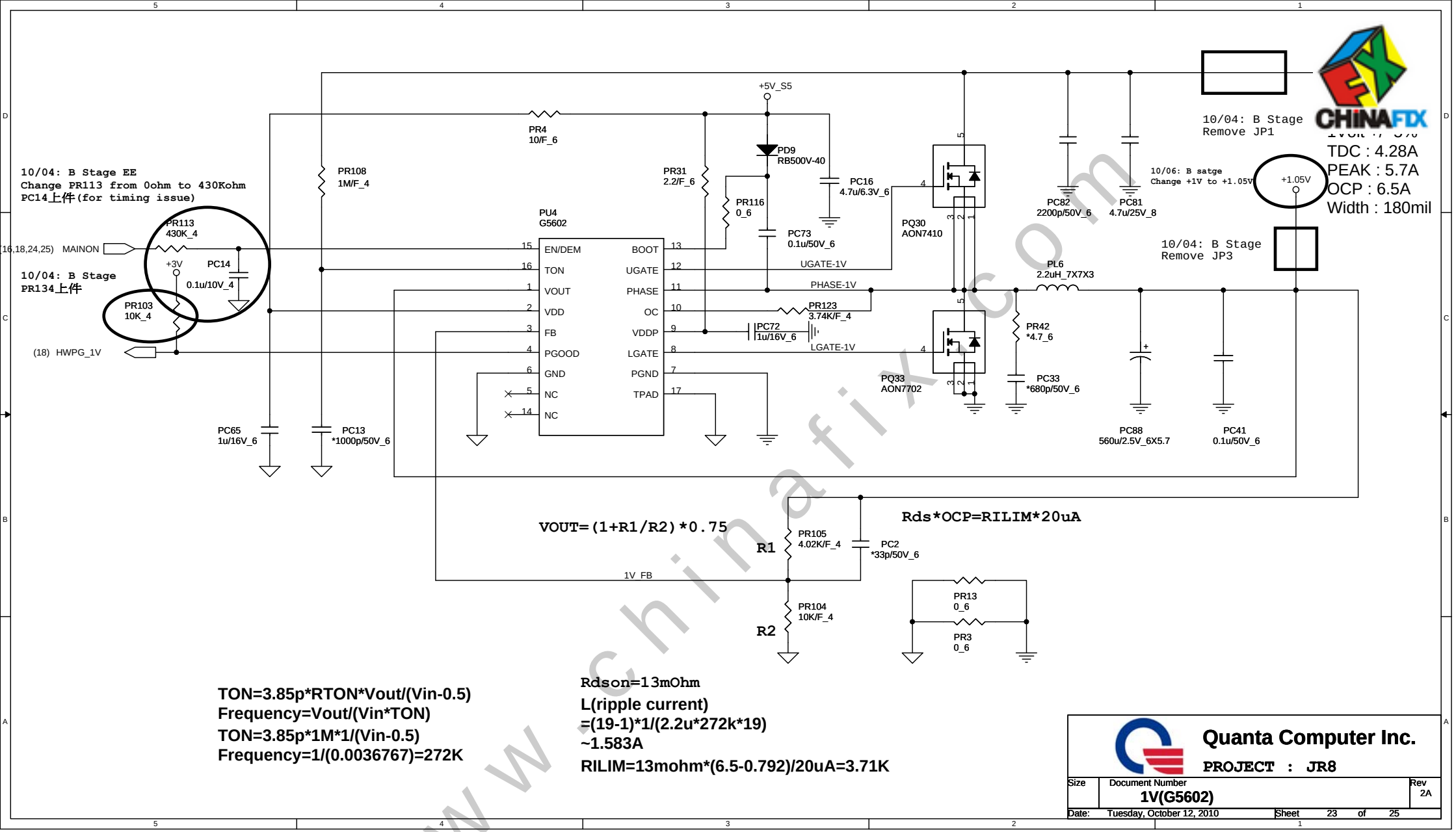

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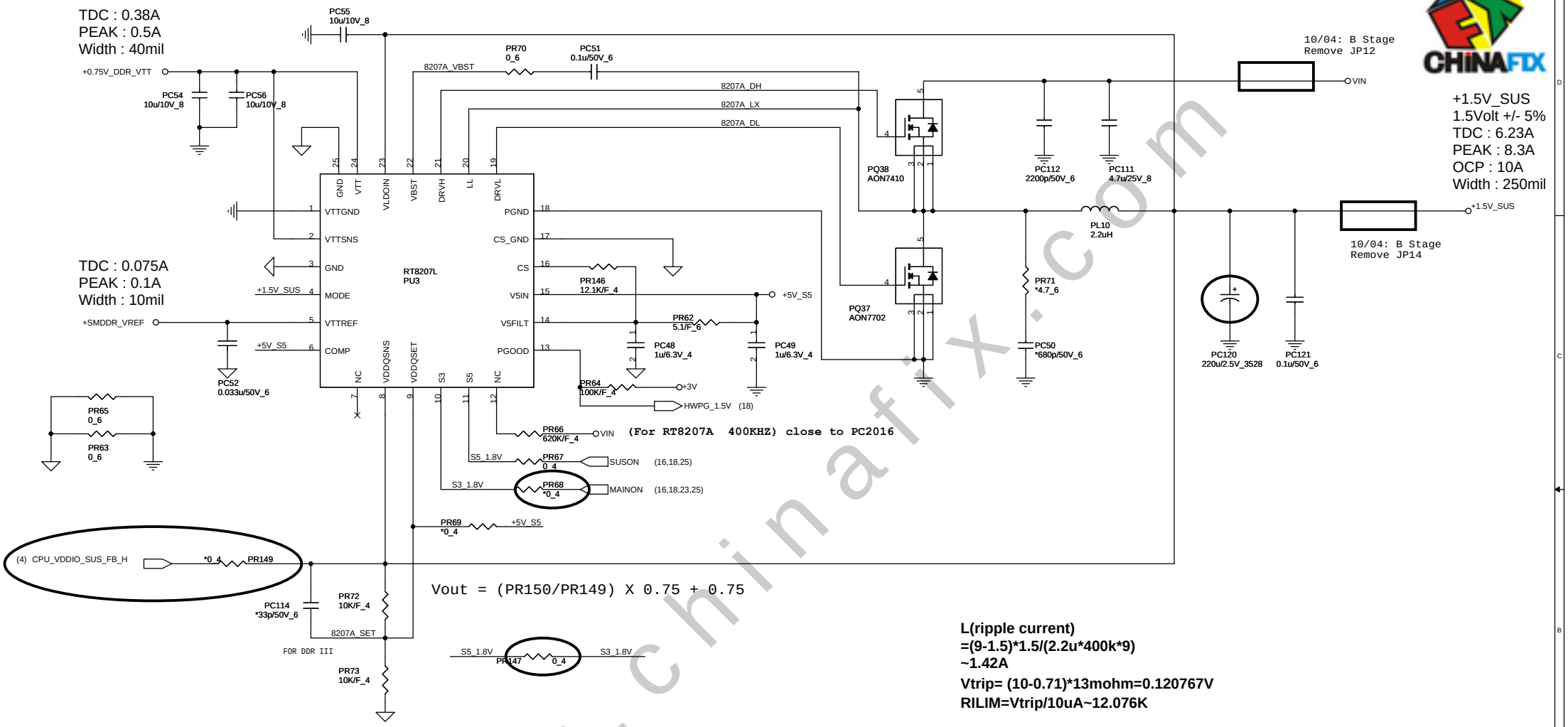

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

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PROJECT : JR8

Size | Document Number: DDR 1.5V(RT8207L) | Rev 2A

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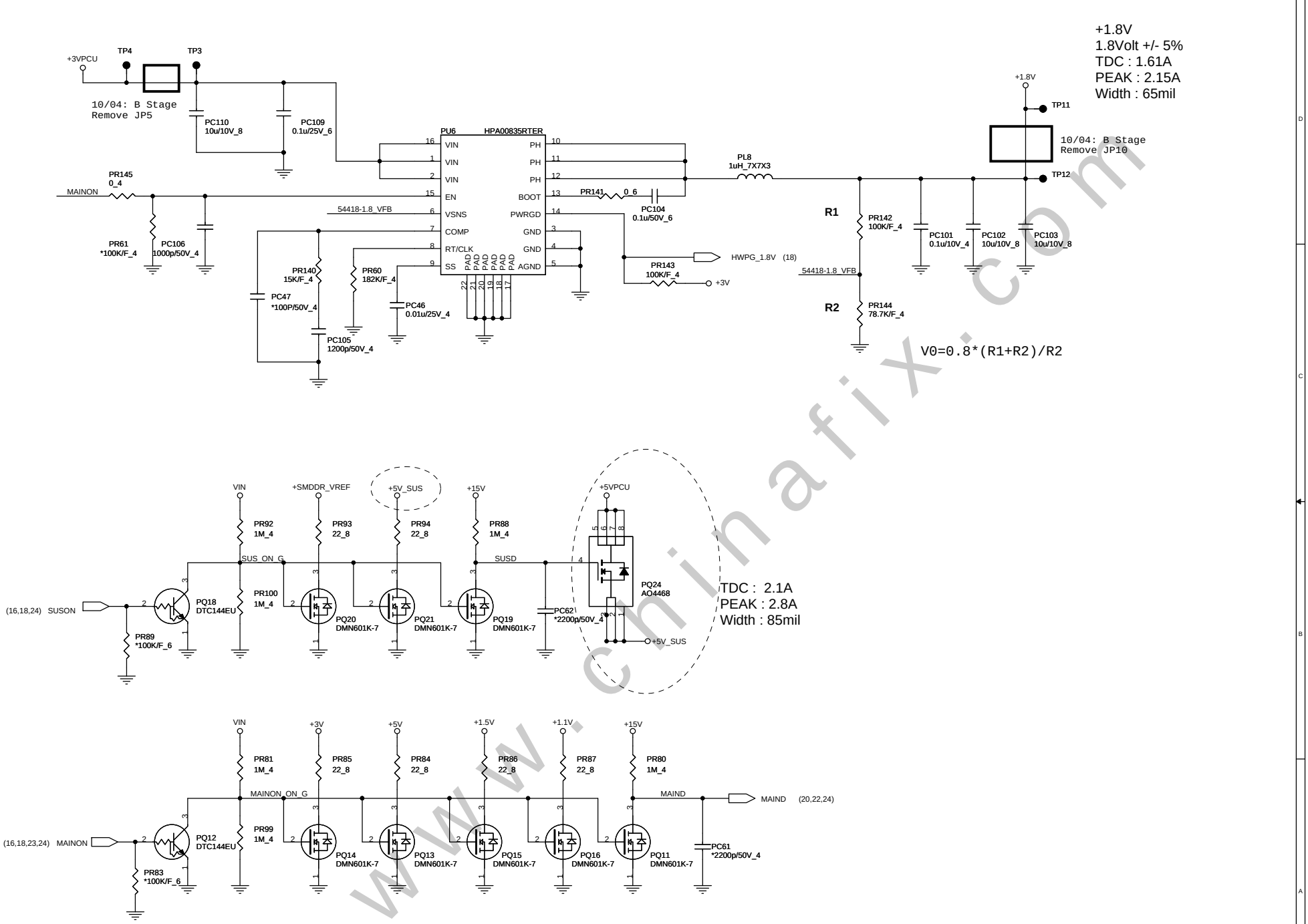

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PROJECT : JR8		
Size	Document Number: Discharge/1.8V	Rev 2A
Date: Tuesday, October 12, 2010	Sheet 25 of 25	

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